COM-HPC-sIDH

User's Guide

intel

COM-HPC™

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ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
0.1	Preliminary release	2023-05-05	CC

Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

The COM-HPC-sIDH is a Server Type COM-HPC Size D module based on Intel® Xeon® D-2700 processors (formerly "Ice Lake-D HCC"). The processor puts an emphasis on longevity and industrial-class reliability, offers up to 20 cores at 3.1GHz boost frequency, and features AVX512-VNNI (Vector Neural Network Instructions) that deliver accelerated AI inferencing performance. Typical industries in need of such high performance, low power characteristics include industrial automation and control, medical ultra sound, image processing and analysis, high-speed video encoding and streaming, predictive traffic analysis, and multi-camera-based AI.

The COM-HPC-sIDH has up to four DIMM sockets supporting up to 256GB (4x 64GB) of DDR4 RDIMM memory, or even higher with LRDIMM. It provides a memory frequency of up to 3200 MT/s, dependent on system configuration.

Selected SKUs features industrial class reliability with extended temperature range operability. Combined with ultra-low latency-focused Intel® Time Coordinated Computing (Intel® TCC) technology, COM-HPC-sIDH is well suited for mission critical, hard real-time, and rugged solutions.

The integrated high speed Ethernet controller inside Intel® Xeon® D-2700 processors provides up to 8x 10G networking with selected PHY on carrier for SFP+ or 10GBASE-T feature, or 4x 25G based on selected PHY on carrier for SFP+, or 10G/25G in KR backplane usage and even up to 40G/50G/100G (TBC) in KR backplane usage. It also includes an onboard 2.5Gigabit Ethernet port with optional Time Sensitive Network (TSN) support.

An optional IPMB via MMC (module management controller, located on module) and a dedicated PCIe lane (PCIe_BMC) are also offered. By connecting these IPMB, dedicated PCIe lane and other management buses, such as eSPI, UART, to the carrier board BMC (for example, AST2500), it allows for out-of-band management.

Inputs/outputs provided include up to two PCIe Gen4 x16 and another two PCIe Gen3 x8 lanes that can be used for AI accelerator and NVMe SSD, four USB 3.0/2.0 ports, two SATA 6Gb/s ports, and 12x GPIO pins. TPM chip is equipped for security-related usage. Optional onboard eMMC is offered by project basis. Support for SMBus, two I^2C. is also available The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

2. Specifications

2.1. Core System

CPU

Intel® Xeon® D-2700 Processor (formerly "Ice Lake-D HCC")

- Intel® Xeon® D-2796TE, 2.0/3.1GHz, 30MB, 20C/40T, 118W (100G Ethernet bandwidth) (eTemp)
- Intel® Xeon® D-2775TE, 2.0/3.1GHz, 25MB, 16C/32T, 100W (100G Ethernet bandwidth) (eTemp)
- Intel® Xeon® D-2752TER, 1.8/2.8GHz, 20MB, 12C/24T, 77W (50G Ethernet bandwidth) (eTemp)
- Intel® Xeon® D-2733NT, 2.1/3.2GHz, 15MB, 8C/16T, 80W (50G Ethernet bandwidth) (Intel QAT)
- Intel® Xeon® D-2712T, 1.9/3.0GHz, 15MB, 4C/8T, 65W (50G Ethernet bandwidth)

Note: Other non-IOTG SKU not listed may be supported by project basis. Please contact our ADLINK local representative.

Memory

Up to 256GB (4x 64GB) DDR4 RDIMM in four DIMM sockets (up to 512 GB by 4x 128GB configuration at LRDIMM, TBC)

Up to 2933 MT/s for D-2796TE/D-2775TE, 2667 MT/s for D-2752TER/D-2733NT/D-2712T

1 DIMM per channel architecture for maximum performance

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 64 (or 32, TBC) MB SPI BIOS, dual BIOS by build option

2.2. Expansion Busses

1 PCI Express x16 Gen4: Lane 16-31 (configurable to 1 x16, 2 x8 or 4 x4)

1 PCI Express x16 Gen4: Lane 32-47 (configurable to 1 x16, 2 x8 or 4 x4)

1 PCI Express x8 Gen3: Lane 0-7 (configurable to 1 x8, 2 x4, 4 x2 or 4 x1. x1 usage at Lane 0, 2, 4, 6)

1 PCI Express x8 Gen3: Lane 8-15 (configurable to 1 x8, 2 x4, 4 x2 or 4 x1. x1 usage at Lane 8, 10, 12, 14)

Additional 1 PCI Express x1 Gen3 (PCIe_BMC) is used for connecting to carrier board BMC

Note: Gen4 support dependent on carrier design.

4 PCI Express Reference Clock:

PCIe_REFCLK0_LO: used for PCIe Lane 0-7 and PCIe_BMC recommended

PCIe_REFCLK0_HI: used for PCIe Lane 8-15 recommended

PCIe_REFCLK1: used for PCIe Lane 16-31 recommended

PCIe_REFCLK2: used for PCIe Lane 32-47 recommended

Note: PCIe 8-11 should be used for the first NVMe instance and PCIe 12-15 should be used for the second NMVe instance. These are recommended by COM-HPC specifications.

Other: SMBus (system), 2x I2C (user, I2C_0, I2C_1, I2C_0 offers ALERT#), eSPI bus

2.3. Ethernet KR

Ethernet Controller

Integrated on SoC

Up to 8x Ethernet KR interfaces with sideband signals

Note: PHY on carrier is required for Optical Fiber / Copper.

Ethernet MAC configuration

		KR_0	KR_1	KR_2	KR_3	KR_4	KR_5	KR_6	KR_7	Note for possible usage
For 100G Ethernet Bandwidth SKU **D-2796TE** **D-2775TE**	**2x 100G**	100G				100G (failover)				Backplane usage
	2x 50G	50G				50G				Backplane usage
	2x 40G	40G				40G				Backplane usage
	4x 25G	25G	25G	25G	25G					Backplane usage SFP+ (1pc, C827 on carrier)
	8x 10G	10G	10G	10G	10G	10G	10G	10G	10G	Backplane usage SFP+ (2pcs, C827 on carrier) 10G BASE-T (2pcs, X557-AT4 on carrier)
For 50G Ethernet Bandwidth SKU **D-2752TER** **D-2733NT** **D-2712T**	**1x 50G**	50G								Backplane usage
	1x 40G	40G								Backplane usage
	4x 10G	10G	10G	10G	10G					Backplane usage SFP+ (1pc, C827 on carrier) 10G BASE-T (1pc, X557-AT4 on carrier)

Note:
1. Firmware for each configuration may differ and is dependent on silicon vendor.
2. Table above shows highest speed supported per lane and can be configured to lower speeds.

3. 10G and 40G support require the use of 4 lanes, while 50G support require 2 lanes.
4. For detailed circuit information between Ethernet Controller, PHY, and firmware, please contact your local ADLINK representative.

2.4. Ethernet NBASE-T

1x NBASE-T port

Onboard Intel® i225 series (IT version) Ethernet Controller

2.5Gbps, 1Gbps and 100/10Mbps connections, 1000BASE-T mode support

IT version supports TSN on Linux OS, with NBASET0_SDP available when TSN support is enabled (TBC)

2.5. Multi I/O and Storage

USB

4x USB3.0/2.0/1.1 (USB 0, 1, 2, 3)

SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

SATA (TBC)

2x SATA 6Gb/s (SATA 0, 1)

Note: HSIO combined bandwidth support can be up to the equivalence of 16 PCIe Gen3 lanes. PCIe lane 0-15, SATA, USB High-speed SSTX/RX pair, NBASE-T, and PCIe_BMC are sourced from HSIO.

On-board Storage

eMMC 5.1, ranges from 32GB/64GB. Build option support by project basis

eMMC as boot-up device for Windows Server 2019 (Yocto support TBC)

GPIO

12x GPIO

GPI with interrupt

UART

2x UART interfaces on module

Console Redirection COM 1 or COM 2 selectable in BIOS

COM Port	Description	IRQ	Address	Console Redirection Support
COM 0	Supported by module (UART 0), via embedded controller	4	0x3F8	Yes
COM 1	Supported by module (UART 1), via embedded controller	5	0x2F8	Yes

Note:

1.The Carrier BMC of ADLINK's reference COM-HPC Server Base offers 2x UART ports and share the physical connector/header with module's UART ports, which can be switched using jumper settings.
2.Carrier BMC_UART_0 and Module_UART_0 connect to a DB9 connector of COM-HPC Server Base. It can be used as BMC Serial over LAN if sourced from Carrier BMC_UART_0. The Carrier BMC_UART_0 IRQ is 9, Address is 0x220.
3.Carrier BMC_UART_1 and Module_UART_1 connect to a pin header of COM-HPC Server Base. It can be used as console module. The Carrier BMC_UART_1 IRQ is 10, Address is 0x228.

2.6. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based)

2.7. SEMA Board controller

Supports: Voltage/current monitoring, power sequence debug support, logistics and forensic information, general purpose I2C, failsafe BIOS (dual BIOS, build opt. support), watchdog timer and fan control

2.8. Remote Management & Module Management Controller (MMC)

An IPMB (Intelligent Platform Management Bus) port and PCIe_BMC lane can work in conjunction with Carrier BMC for remote management applications, build option, supported by project basis

IPMB

It is offered by MMC (Module Management Controller) and is used for the connection between Carrier BMC and module MMC, build option

PCIe_BMC

It is a dedicated PCIe x1 lane for Carrier BMC, lets Carrier BMC emulate graphics card features and is mainly used for KVM

MMC, Module Management Controller

It works in conjunction with Carrier BMC through IPMB and/or UART, I2C

Reacts with Carrier BMC, e.g. forwarding COM-HPC module's temperature, voltage, FAN speed, board information to Carrier BMC.

Information is either obtained by MMC itself through GPIO/I2C or by communication with SEMA Board Controller. Remotely power on/off COM-HPC module through Carrier BMC/MMC is also supported

2.9. Debug

40-pin flat cable connector for use with DB40-HPC debug module

Supports BIOS POST code LED, SEMA Board Controller access, Module Management Controller access, SPI BIOS flashing, internal power rail test points, debug LEDs

2.10. Power

Power Modes: AT mode

Standard Voltage Input: AT: 12V±5%Power Management: ACPI 5.0 compliant

Power States: S0, S5 (WoL S5)

2.11. Mechanical and Environmental

Form Factor and Specification

PICMG COM-HPC Rev 1.1, Server Type, Size D 160 x 160 mm

Operating Temperature

Standard	0°C to 60°C (Standard Voltage Input)	Storage: -20°C to 80°C
Extreme Rugged (Selected SoC SKUs)	-40°C to 85°C (Standard Voltage Input)	Storage: -40°C to 85°C

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

3. Block Diagram

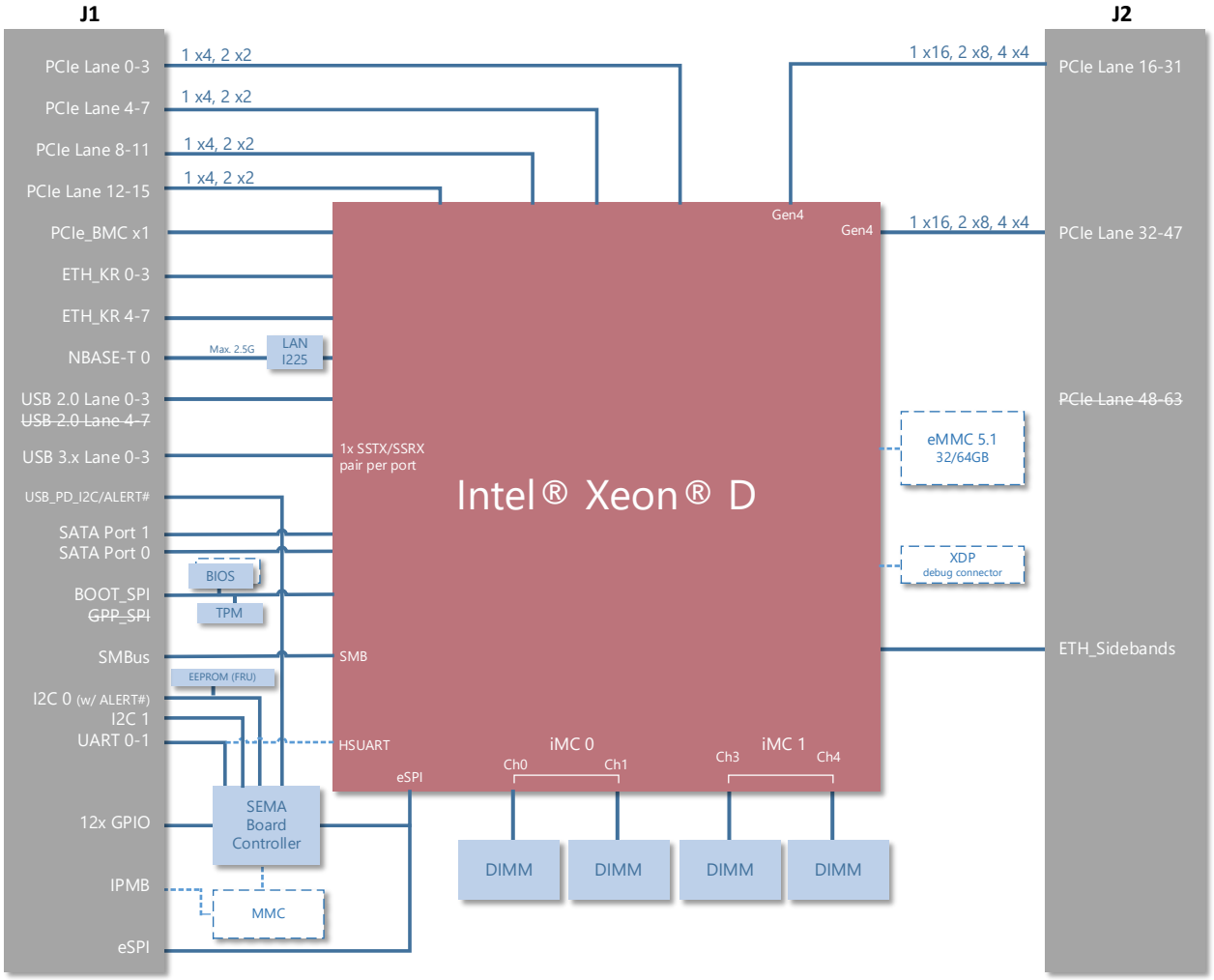


Figure 1 – Module function diagram

4. Pinout and Signal Descriptions

4.1. Pin Summary

The table below is a comprehensive list of all signal pins supported on the dual 400-pin COM-HPC connectors as defined for Server Type in the PICMG COM-HPC R1.1 specification. Signals described in the specification but not supported on the COM-HPC-sIDH are marked by ~~STRIKETHROUGH.~~

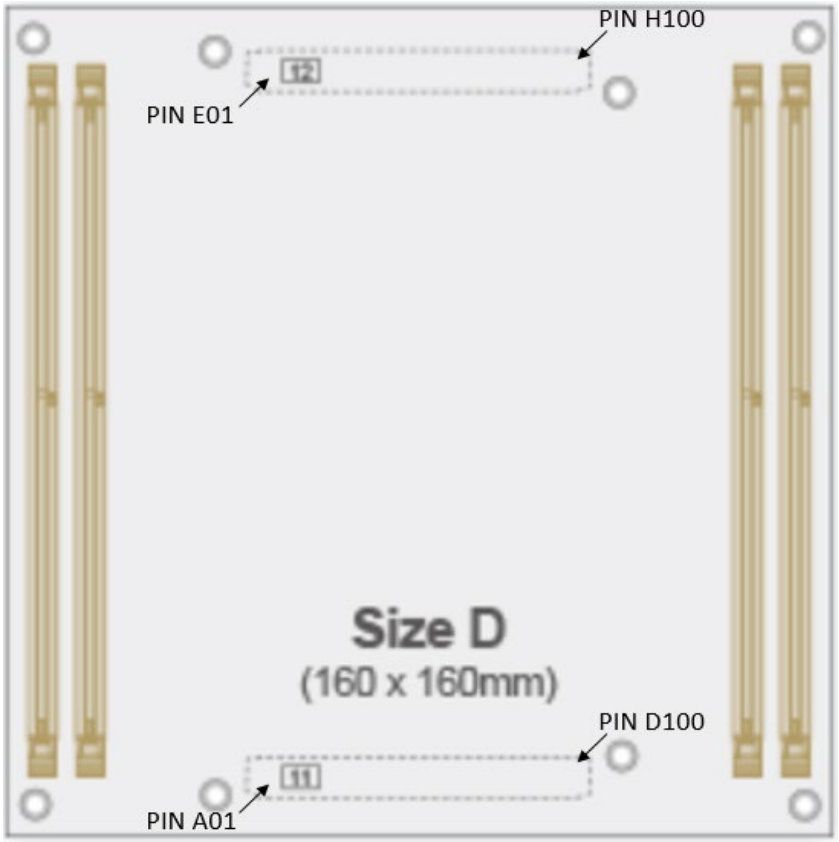


Figure 2 - Module rear side row and pin numbering

Row A			Row B			Row C			Row D	
A1	VCC		B1	VCC		C1	VCC		D1	VCC
A2	VCC		B2	PWRBTN#		C2	RSTBTN#		D2	VCC
A3	VCC		B3	VCC		C3	VCC		D3	VCC
A4	VCC		B4	THERMTRIP#		C4	CARRIER_HOT#		D4	VCC
A5	VCC		B5	VCC		C5	VCC		D5	VCC
A6	VCC		B6	~~TAMPER#~~		C6	VIN_PWR_OK		D6	VCC
A7	VCC		B7	VCC		C7	VCC		D7	VCC
A8	VCC		B8	SUS_S3#		C8	SUS_S4_S5#		D8	VCC
A9	VCC		B9	VCC		C9	VCC		D9	VCC
A10	GND		B10	WD_STROBE#		C10	GND		D10	WAKE0#
A11	BATLOW#		B11	WD_OUT		C11	FAN_PWMOUT		D11	WAKE1#
A12	PLTRST#		B12	GND		C12	FAN_TACHIN		D12	GND
A13	GND		B13	~~USB5-~~		C13	GND		D13	USB1-
A14	~~USB7-~~		B14	~~USB5+~~		C14	USB3-		D14	USB1+
A15	~~USB7+~~		B15	GND		C15	USB3+		D15	GND
A16	GND		B16	~~USB4-~~		C16	GND		D16	USB0-
A17	~~USB6-~~		B17	~~USB4+~~		C17	USB2-		D17	USB0+
A18	~~USB6+~~		B18	GND		C18	USB2+		D18	GND
A19	GND		B19	RSVD		C19	GND		D19	ETH0_RX-
A20	ETH4_RX-		B20	RSVD		C20	ETH0_TX-		D20	ETH0_RX+
A21	ETH4_RX+		B21	RSVD		C21	ETH0_TX+		D21	GND
A22	GND		B22	RSVD		C22	GND		D22	ETH1_RX-
A23	ETH5_RX-		B23	RSVD		C23	ETH1_TX-		D23	ETH1_RX+
A24	ETH5_RX+		B24	VCC_5V_SBY		C24	ETH1_TX+		D24	GND
A25	GND		B25	~~USB67_OC#~~		C25	GND		D25	ETH2_RX-
A26	ETH6_RX-		B26	~~USB45_OC#~~		C26	ETH2_TX-		D26	ETH2_RX+
A27	ETH6_RX+		B27	USB23_OC#		C27	ETH2_TX+		D27	GND
A28	GND		B28	USB01_OC#		C28	GND		D28	ETH3_RX-
A29	ETH7_RX-		B29	~~SML1_CLK~~		C29	ETH3_TX-		D29	ETH3_RX+
A30	ETH7_RX+		B30	~~SML1_DAT~~		C30	ETH3_TX+		D30	GND
A31	GND		B31	PMCALERT#		C31	GND		D31	USB3_SSTX-
A32	RSVD		B32	~~SML0_CLK~~		C32	USB3_SSRX-		D32	USB3_SSTX+
A33	RSVD		B33	~~SML0_DAT~~		C33	USB3_SSRX+		D33	GND
A34	GND		B34	~~USB_PD_ALERT#~~		C34	GND		D34	USB2_SSTX-
A35	ETH4_TX-		B35	USB_PD_I2C_CLK		C35	USB2_SSRX-		D35	USB2_SSTX+
A36	ETH4_TX+		B36	USB_PD_I2C_DAT		C36	USB2_SSRX+		D36	GND

Row A			Row B			Row C			Row D	
A37	GND		B37	~~USB_RT_ENA~~		C37	GND		D37	USB1_SSTX0-
A38	ETH5_TX-		B38	~~USB1_LSRX~~		C38	USB1_SSRX0-		D38	USB1_SSTX0+
A39	ETH5_TX+		B39	~~USB1_LSTX~~		C39	USB1_SSRX0+		D39	GND
A40	GND		B40	~~USB0_LSRX~~		C40	GND		D40	~~USB1_SSTX1-~~
A41	ETH6_TX-		B41	~~USB0_LSTX~~		C41	~~USB1_SSRX1-~~		D41	~~USB1_SSTX1+~~
A42	ETH6_TX+		B42	GND		C42	~~USB1_SSRX1+~~		D42	GND
A43	GND		B43	~~USB0_AUX-~~		C43	GND		D43	USB0_SSTX0-
A44	ETH7_TX-		B44	~~USB0_AUX+~~		C44	USB0_SSRX0-		D44	USB0_SSTX0+
A45	ETH7_TX+		B45	RSVD		C45	USB0_SSRX0+		D45	GND
A46	GND		B46	RSVD		C46	GND		D46	~~USB0_SSTX1-~~
A47	~~USB1_AUX-~~		B47	VCC_BOOT_SPI		C47	~~USB0_SSRX1-~~		D47	~~USB0_SSTX1+~~
A48	~~USB1_AUX+~~		B48	BOOT_SPI_CS#		C48	~~USB0_SSRX1+~~		D48	GND
A49	GND		B49	BSEL0		C49	GND		D49	SATA0_RX- *
A50	eSPI_IO0		B50	BSEL1		C50	BOOT_SPI_IO0		D50	SATA0_RX+ *
A51	eSPI_IO1		B51	BSEL2		C51	BOOT_SPI_IO1		D51	GND
A52	eSPI_IO2		B52	eSPI_ALERT0#		C52	~~BOOT_SPI_IO2~~		D52	SATA0_TX- *
A53	eSPI_IO3		B53	~~eSPI_ALERT1#~~		C53	~~BOOT_SPI_IO3~~		D53	SATA0_TX+ *
A54	eSPI_CLK		B54	eSPI_CS0#		C54	BOOT_SPI_CLK		D54	GND
A55	GND		B55	~~eSPI_CS1#~~		C55	GND		D55	SATA1_RX- *
A56	PCIe_CLKREQ0_LO#		B56	eSPI_RST#		C56	PCIe_REFCLK0_HI-		D56	SATA1_RX+*
A57	PCIe_CLKREQ0_HI#		B57	GND		C57	PCIe_REFCLK0_HI+		D57	GND
A58	GND		B58	PCIe_BMC_RX-		C58	GND		D58	SATA1_TX- *
A59	PCIe_BMC_TX-		B59	PCIe_BMC_RX+		C59	PCIe_REFCLK0_LO-		D59	SATA1_TX+*
A60	PCIe_BMC_TX+		B60	GND		C60	PCIe_REFCLK0_LO+		D60	GND
A61	GND		B61	PCIe08_RX-		C61	GND		D61	PCIe00_TX-
A62	PCIe08_TX-		B62	PCIe08_RX+		C62	PCIe00_RX-		D62	PCIe00_TX+
A63	PCIe08_TX+		B63	GND		C63	PCIe00_RX+		D63	GND
A64	GND		B64	PCIe09_RX-		C64	GND		D64	PCIe01_TX-
A65	PCIe09_TX-		B65	PCIe09_RX+		C65	PCIe01_RX-		D65	PCIe01_TX+
A66	PCIe09_TX+		B66	GND		C66	PCIe01_RX+		D66	GND
A67	GND		B67	PCIe10_RX-		C67	GND		D67	PCIe02_TX-
A68	PCIe10_TX-		B68	PCIe10_RX+		C68	PCIe02_RX-		D68	PCIe02_TX+
A69	PCIe10_TX+		B69	GND		C69	PCIe02_RX+		D69	GND
A70	GND		B70	PCIe11_RX-		C70	GND		D70	PCIe03_TX-
A71	PCIe11_TX-		B71	PCIe11_RX+		C71	PCIe03_RX-		D71	PCIe03_TX+
A72	PCIe11_TX+		B72	GND		C72	PCIe03_RX+		D72	GND

Row A			Row B			Row C			Row D	
A73	GND		B73	PCIe12_RX-		C73	GND		D73	PCIe04_TX-
A74	PCIe12_TX-		B74	PCIe12_RX+		C74	PCIe04_RX-		D74	PCIe04_TX+
A75	PCIe12_TX+		B75	GND		C75	PCIe04_RX+		D75	GND
A76	GND		B76	PCIe13_RX-		C76	GND		D76	PCIe05_TX-
A77	PCIe13_TX-		B77	PCIe13_RX+		C77	PCIe05_RX-		D77	PCIe05_TX+
A78	PCIe13_TX+		B78	GND		C78	PCIe05_RX+		D78	GND
A79	GND		B79	PCIe14_RX-		C79	GND		D79	PCIe06_TX-
A80	PCIe14_TX-		B80	PCIe14_RX+		C80	PCIe06_RX-		D80	PCIe06_TX+
A81	PCIe14_TX+		B81	GND		C81	PCIe06_RX+		D81	GND
A82	GND		B82	PCIe15_RX-		C82	GND		D82	PCIe07_TX-
A83	PCIe15_TX-		B83	PCIe15_RX+		C83	PCIe07_RX-		D83	PCIe07_TX+
A84	PCIe15_TX+		B84	GND		C84	PCIe07_RX+		D84	GND
A85	GND		B85	~~TEST#~~		C85	GND		D85	NBASET0_MDI0-
A86	VCC_RTC		B86	RSMRST_OUT#		C86	SMB_CLK		D86	NBASET0_MDI0+
A87	SUS_CLK		B87	UART1_TX		C87	SMB_DAT		D87	GND
A88	GPIO_00		B88	UART1_RX		C88	SMB_ALERT#		D88	NBASET0_MDI1-
A89	GPIO_01		B89	UART1_RTS#		C89	UART0_TX		D89	NBASET0_MDI1+
A90	GPIO_02		B90	UART1_CTS#		C90	UART0_RX		D90	GND
A91	GPIO_03		B91	IPMB_CLK		C91	UART0_RTS#		D91	NBASET0_MDI2-
A92	GPIO_04		B92	IPMB_DAT		C92	UART0_CTS#		D92	NBASET0_MDI2+
A93	GPIO_05		B93	~~GPSPI_MOSI~~		C93	I2C0_CLK		D93	GND
A94	GPIO_06		B94	~~GPSPI_MISO~~		C94	I2C0_DAT		D94	NBASET0_MDI3-
A95	GPIO_07		B95	~~GPSPI_CS0#~~		C95	I2C0_ALERT#		D95	NBASET0_MDI3+
A96	GPIO_08		B96	~~GPSPI_CS1#~~		C96	I2C1_CLK		D96	GND
A97	GPIO_09		B97	~~GPSPI_CS2#~~		C97	I2C1_DAT		D97	NBASET0_LINK_MAX#
A98	GPIO_10		B98	~~GPSPI_CS3#~~		C98	NBASET0_SDP *		D98	NBASET0_LINK_MID#
A99	GPIO_11		B99	~~GPSPI_CLK~~		C99	~~NBASET0_CTREF~~		D99	NBASET0_LINK_ACT#
A100	TYPE0		B100	~~GPSPI_ALERT#~~		C100	TYPE1		D100	TYPE2

Row E			Row F			Row G			Row H	
E1	~~RAPID_SHUTDOWN~~		F1	ETH2_SDP		G1	VCC_5V_SBY		H1	RSVD
E2	GND		F2	ETH3_SDP		G2	~~FUSA_STATUS0~~		H2	RSVD
E3	RSVD		F3	~~ETH4_SDP~~		G3	~~FUSA_STATUS1~~		H3	RSVD
E4	RSVD		F4	~~ETH5_SDP~~		G4	~~FUSA_ALERT#~~		H4	RSVD
E5	GND		F5	~~ETH6_SDP~~		G5	~~FUSA_SPI_CS#~~		H5	RSVD
E6	RSVD		F6	~~ETH7_SDP~~		G6	~~FUSA_SPI_CLK~~		H6	RSVD
E7	RSVD		F7	ETH4-7_I2C_CLK		G7	~~FUSA_SPI_MISO~~		H7	RSVD
E8	GND		F8	ETH4-7_I2C_DAT		G8	~~FUSA_SPI_MOSI~~		H8	RSVD
E9	RSVD		F9	ETH4-7_INT#		G9	~~FUSA_SPI_ALERT~~		H9	RSVD
E10	RSVD		F10	ETH4-7_MDIO_CLK		G10	~~FUSA_VOLTAGE_ERR#~~		H10	RSVD
E11	GND		F11	ETH4-7_MDIO_DAT		G11	~~PROCHOT#~~		H11	RSVD
E12	RSVD		F12	~~ETH4-7_PHY_INT#~~		G12	~~CATERR#~~		H12	RSVD
E13	RSVD		F13	ETH4-7_PHY_RST#		G13	RSVD		H13	RSVD
E14	GND		F14	ETH4-7_PRSNT#		G14	GND		H14	RSVD
E15	RSVD		F15	RSVD		G15	RSVD		H15	RSVD
E16	RSVD		F16	RSVD		G16	RSVD		H16	RSVD
E17	GND		F17	RSVD		G17	RSVD		H17	RSVD
E18	RSVD		F18	RSVD		G18	RSVD		H18	RSVD
E19	RSVD		F19	GND		G19	RSVD		H19	GND
E20	GND		F20	PCIe32_RX-		G20	GND		H20	PCIe40_TX-
E21	PCIe32_TX-		F21	PCIe32_RX+		G21	PCIe40_RX-		H21	PCIe40_TX+
E22	PCIe32_TX+		F22	GND		G22	PCIe40_RX+		H22	GND
E23	GND		F23	PCIe33_RX-		G23	GND		H23	PCIe41_TX-
E24	PCIe33_TX-		F24	PCIe33_RX+		G24	PCIe41_RX-		H24	PCIe41_TX+
E25	PCIe33_TX+		F25	GND		G25	PCIe41_RX+		H25	GND
E26	GND		F26	PCIe34_RX-		G26	GND		H26	PCIe42_TX-
E27	PCIe34_TX-		F27	PCIe34_RX+		G27	PCIe42_RX-		H27	PCIe42_TX+
E28	PCIe34_TX+		F28	GND		G28	PCIe42_RX+		H28	GND
E29	GND		F29	PCIe35_RX-		G29	GND		H29	PCIe43_TX-
E30	PCIe35_TX-		F30	PCIe35_RX+		G30	PCIe43_RX-		H30	PCIe43_TX+
E31	PCIe35_TX+		F31	GND		G31	PCIe43_RX+		H31	GND
E32	GND		F32	PCIe36_RX-		G32	GND		H32	PCIe44_TX-
E33	PCIe36_TX-		F33	PCIe36_RX+		G33	PCIe44_RX-		H33	PCIe44_TX+
E34	PCIe36_TX+		F34	GND		G34	PCIe44_RX+		H34	GND
E35	GND		F35	PCIe37_RX-		G35	GND		H35	PCIe45_TX-
E36	PCIe37_TX-		F36	PCIe37_RX+		G36	PCIe45_RX-		H36	PCIe45_TX+

Row E			Row F			Row G			Row H	
E37	PCIe37_TX+		F37	GND		G37	PCIe45_RX+		H37	GND
E38	GND		F38	PCIe38_RX-		G38	GND		H38	PCIe46_TX-
E39	PCIe38_TX-		F39	PCIe38_RX+		G39	PCIe46_RX-		H39	PCIe46_TX+
E40	PCIe38_TX+		F40	GND		G40	PCIe46_RX+		H40	GND
E41	GND		F41	PCIe39_RX-		G41	GND		H41	PCIe47_TX-
E42	PCIe39_TX-		F42	PCIe39_RX+		G42	PCIe47_RX-		H42	PCIe47_TX+
E43	PCIe39_TX+		F43	GND		G43	PCIe47_RX+		H43	GND
E44	GND		F44	PCIe16_RX-		G44	GND		H44	PCIe24_TX-
E45	PCIe16_TX-		F45	PCIe16_RX+		G45	PCIe24_RX-		H45	PCIe24_TX+
E46	PCIe16_TX+		F46	GND		G46	PCIe24_RX+		H46	GND
E47	GND		F47	PCIe17_RX-		G47	GND		H47	PCIe25_TX-
E48	PCIe17_TX-		F48	PCIe17_RX+		G48	PCIe25_RX-		H48	PCIe25_TX+
E49	PCIe17_TX+		F49	GND		G49	PCIe25_RX+		H49	GND
E50	GND		F50	PCIe18_RX-		G50	GND		H50	PCIe26_TX-
E51	PCIe18_TX-		F51	PCIe18_RX+		G51	PCIe26_RX-		H51	PCIe26_TX+
E52	PCIe18_TX+		F52	GND		G52	PCIe26_RX+		H52	GND
E53	GND		F53	PCIe19_RX-		G53	GND		H53	PCIe27_TX-
E54	PCIe19_TX-		F54	PCIe19_RX+		G54	PCIe27_RX-		H54	PCIe27_TX+
E55	PCIe19_TX+		F55	GND		G55	PCIe27_RX+		H55	GND
E56	GND		F56	PCIe20_RX-		G56	GND		H56	PCIe28_TX-
E57	PCIe20_TX-		F57	PCIe20_RX+		G57	PCIe28_RX-		H57	PCIe28_TX+
E58	PCIe20_TX+		F58	GND		G58	PCIe28_RX+		H58	GND
E59	GND		F59	PCIe21_RX-		G59	GND		H59	PCIe29_TX-
E60	PCIe21_TX-		F60	PCIe21_RX+		G60	PCIe29_RX-		H60	PCIe29_TX+
E61	PCIe21_TX+		F61	GND		G61	PCIe29_RX+		H61	GND
E62	GND		F62	PCIe22_RX-		G62	GND		H62	PCIe30_TX-
E63	PCIe22_TX-		F63	PCIe22_RX+		G63	PCIe30_RX-		H63	PCIe30_TX+
E64	PCIe22_TX+		F64	GND		G64	PCIe30_RX+		H64	GND
E65	GND		F65	PCIe23_RX-		G65	GND		H65	PCIe31_TX-
E66	PCIe23_TX-		F66	PCIe23_RX+		G66	PCIe31_RX-		H66	PCIe31_TX+
E67	PCIe23_TX+		F67	GND		G67	PCIe31_RX+		H67	GND
E68	GND		F68	~~PCIe48_RX-~~		G68	GND		H68	~~PCIe56_TX-~~
E69	~~PCIe48_TX-~~		F69	~~PCIe48_RX+~~		G69	~~PCIe56_RX-~~		H69	~~PCIe56_TX+~~
E70	~~PCIe48_TX+~~		F70	GND		G70	~~PCIe56_RX+~~		H70	GND
E71	GND		F71	~~PCIe49_RX-~~		G71	GND		H71	~~PCIe57_TX-~~
E72	~~PCIe49_TX-~~		F72	~~PCIe49_RX+~~		G72	~~PCIe57_RX-~~		H72	~~PCIe57_TX+~~

Row E			Row F			Row G			Row H	
E73	~~PCIe49_TX+~~		F73	GND		G73	~~PCIe57_RX+~~		H73	GND
E74	GND		F74	~~PCIe50_RX-~~		G74	GND		H74	~~PCIe58_TX-~~
E75	~~PCIe50_TX-~~		F75	~~PCIe50_RX+~~		G75	~~PCIe58_RX-~~		H75	~~PCIe58_TX+~~
E76	~~PCIe50_TX+~~		F76	GND		G76	~~PCIe58_RX+~~		H76	GND
E77	GND		F77	~~PCIe51_RX-~~		G77	GND		H77	~~PCIe59_TX-~~
E78	~~PCIe51_TX-~~		F78	~~PCIe51_RX+~~		G78	~~PCIe59_RX-~~		H78	~~PCIe59_TX+~~
E79	~~PCIe51_TX+~~		F79	GND		G79	~~PCIe59_RX+~~		H79	GND
E80	GND		F80	~~PCIe52_RX-~~		G80	GND		H80	~~PCIe60_TX-~~
E81	~~PCIe52_TX-~~		F81	~~PCIe52_RX+~~		G81	~~PCIe60_RX-~~		H81	~~PCIe60_TX+~~
E82	~~PCIe52_TX+~~		F82	GND		G82	~~PCIe60_RX+~~		H82	GND
E83	GND		F83	~~PCIe53_RX-~~		G83	GND		H83	~~PCIe61_TX-~~
E84	~~PCIe53_TX-~~		F84	~~PCIe53_RX+~~		G84	~~PCIe61_RX-~~		H84	~~PCIe61_TX+~~
E85	~~PCIe53_TX+~~		F85	GND		G85	~~PCIe61_RX+~~		H85	GND
E86	GND		F86	~~PCIe54_RX-~~		G86	GND		H86	~~PCIe62_TX-~~
E87	~~PCIe54_TX-~~		F87	~~PCIe54_RX+~~		G87	~~PCIe62_RX-~~		H87	~~PCIe62_TX+~~
E88	~~PCIe54_TX+~~		F88	GND		G88	~~PCIe62_RX+~~		H88	GND
E89	GND		F89	~~PCIe55_RX-~~		G89	GND		H89	~~PCIe63_TX-~~
E90	~~PCIe55_TX-~~		F90	~~PCIe55_RX+~~		G90	~~PCIe63_RX-~~		H90	~~PCIe63_TX+~~
E91	~~PCIe55_TX+~~		F91	GND		G91	~~PCIe63_RX+~~		H91	GND
E92	GND		F92	PCIe_REFCLK2-		G92	GND		H92	~~PCIe_REFCLKIN0-~~
E93	PCIe_REFCLK1-		F93	PCIe_REFCLK2+		G93	~~PCIe_REFCLK3-~~		H93	~~PCIe_REFCLKIN0+~~
E94	PCIe_REFCLK1+		F94	GND		G94	~~PCIe_REFCLK3+~~		H94	GND
E95	GND		F95	PCIe_CLKREQ3#		G95	GND		H95	~~PCIe_REFCLKIN1-~~
E96	PCIe_CLKREQ1#		F96	ETH0-3_PRSNT#		G96	ETH0-3_I2C_CLK		H96	~~PCIe_REFCLKIN1+~~
E97	PCIe_CLKREQ2#		F97	ETH0-3_PHY_RST#		G97	ETH0-3_I2C_DAT		H97	GND
E98	~~PCIe_CLKREQ_OUT0#~~		F98	ETH0_SDP		G98	~~ETH0-3_PHY_INT#~~		H98	ETH0-3_MDIO_CLK
E99	~~PCIe_CLKREQ_OUT1#~~		F99	ETH1_SDP		G99	ETH0-3_INT#		H99	ETH0-3_MDIO_DAT
E100	~~PCIe_PERST_IN0#~~		F100	~~PCIe_PERST_IN1#~~		G100	~~PCIe_WAKE_OUT0#~~		H100	~~PCIe_WAKE_OUT1#~~

Note: NBASET0_SDP depends on LAN controller SK.

4.2. Signal Terminology Descriptions

Meaning of the terms used in signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

4.3. Signal Descriptions on J1/J2 Connectors

4.3.1 Ethernet KR

KR interface are defined for COM-HPC. For these ports, the Ethernet MACs are located on COM-HPC module. PHYs (if used) are on the Carrier. COM-HPC support both of MDIO and I2C control interfaces for the PHYs. The MDIO and I2C control interfaces are grouped into quads, for KR ports 0:3 and ports 4:7

Name	Pin #	Description	I/O	PU / PD	Comment
ETH0_TX- ETH0_TX+ ETH1_TX- ETH1_TX+ ETH2_TX- ETH2_TX+ ETH3_TX- ETH3_TX+	C20 C21 C23 C24 C26 C27 C29 C30	Ethernet KR ports, transmit output differential pairs.	O KR		AC coupled off Module
ETH0_RX- ETH0_RX+ ETH1_RX- ETH1_RX+ ETH2_RX- ETH2_RX+ ETH3_RX- ETH3_RX+	D19 D20 D22 D23 D25 D26 D28 D29	Ethernet KR ports, receive input differential pairs.	I KR		AC coupled off Module
ETH0-3_MDIO_DAT	H99	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3	I/O 3.3VSB	PU 1K 3.3VSB	
ETH0-3_MDIO_CLK	H98	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 3	O 3.3VSB	PU 1K 3.3VSB	
ETH0-3_INT#	G99	Active low interrupt signal from IO Port expanders for ETH ports 0 to 3	I 3.3VSB	PU 10K 3.3VSB	
~~ETH0-3_PHY_INT#~~	~~G98~~	~~Active low PHY interrupt signal from ETH ports 0 to 3~~	~~I~~ ~~3.3VSB~~	~~PU 1K~~ ~~3.3VSB~~	Not supported

ETH0-3_PHY_RST#	F97	Active low output PHY reset signal for ETH ports 0 to 3.	O 3.3VSB	PU 4.7K 3.3VSB	
ETH0-3_I2C_DAT	G97	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 0 to 3 and for serialized status information (e.g. LED states)..	I/O OD 3.3VSB	PU 10K 3.3VSB	
ETH0-3_I2C_CLK	G96	The I2C clock signals associated with ETH0-3 I2C data lines in the row above.	I/O OD 3.3VSB	PU 10K 3.3VSB	
ETH0_SDP ETH1_SDP ETH2_SDP ETH3_SDP	F98 F99 F1 F2	Software-Definable Pins. Can also be used for IEEE1588 support such as a PPS signal.	I/O 3.3VSB		
ETH0-3_PRSNT#	H96	Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signaling on ETH0 through ETH3. If the entire KR quad is not supported it should fill from ETH0 on up.	I 3.3VSB	PU 10K 3.3VSB	

Name	Pin #	Description	I/O	PU / PD	Comment
ETH4_TX- ETH4_TX+ ETH5_TX- ETH5_TX+ ETH6_TX- ETH6_TX+ ETH7_TX- ETH7_TX+	A35 A36 A38 A39 A41 A42 A44 A45	Ethernet KR ports, transmit output differential pairs.	O KR		AC coupled off Module
ETH4_RX- ETH4_RX+ ETH5_RX- ETH5_RX+ ETH6_RX- ETH6_RX+ ETH7_RX- ETH7_RX+	A20 A21 A23 A24 A26 A27 A29 A30	Ethernet KR ports, receive input differential pairs.	I KR		AC coupled off Module
ETH4-7_MDIO_DAT	F11	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 4 to 7	I/O 3.3VSB	PU 1K 3.3VSB	

ETH4-7_MDIO_CLK	F10	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 4 to 7	O 3.3VSB	PU 1K 3.3VSB	
ETH4-7_INT#	F9	Active low interrupt signal from IO Port expanders for ETH ports 4 to 7	I 3.3VSB	PU 4.7K 3.3VSB	
~~ETH4-7_PHY_INT#~~	~~F12~~	~~Active low PHY interrupt signal from ETH ports 4 to 7~~	~~I~~ ~~3.3VSB~~		Not supported
ETH4-7_PHY_RST#	F13	Active low output PHY reset signal for ETH ports 4 to 7.	O 3.3VSB	PU 4.7K 3.3VSB	
ETH4-7_I2C_DAT	F8	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 4 to 7 and for serialized status information (e.g. LED states)..	I/O OD 3.3VSB	PU 10K 3.3VSB	
ETH4-7_I2C_CLK	F7	The I2C clock signals associated with ETH4-7 I2C data lines in the row above.	I/O OD 3.3VSB	PU 10K 3.3VSB	
ETH4_SDP ETH5_SDP ETH6_SDP ETH7_SDP	F3 F4 F5 F6	Software-Definable Pins. Can also be used for IEEE1588 support such as a PPS signal.	I/O 3.3VSB		
ETH4-7_PRSNT#	F14	Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signaling on ETH4 through ETH7. If the entire KR quad is not supported it should fill from ETH4 on up.	I 3.3VSB	PU 10K 3.3VSB	

4.3.2 NBASE-T Ethernet

Magnetics are on the Carrier board. The COM-HPC module shall be capable of 1000BASE-T mode.

Name	Pin #	Description	I/O	PU / PD	Comment
NBASET0_MDI0- NBASET0_MDI0+ NBASET0_MDI1- NBASET0_MDI1+ NBASET0_MDI2- NBASET0_MDI2+	D85 D86 D88 D89 D91 D92	Ethernet Controller 1: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10Gbps, 1Gbps, 100Mbps and 10 Mbps modes. Some pairs are unused in some modes, per the following:	I/O Analog		Twisted pair signals for external transformer.

<table>
<tr>
<td>NBASET0_MDI3-
NBASET0_MDI3+</td>
<td>D93
D94</td>
<td>
<table>
<tr><td></td><td>10000BASE-T
1000BASE-T</td><td>100BASE-TX</td><td>10BASE-T</td></tr>
<tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr>
<tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr>
<tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr>
<tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr>
</table>
</td>
<td></td><td></td><td></td>
</tr>
<tr>
<td>NBASET0_LINK_ACT#</td>
<td>D99</td>
<td>NBASE-T Ethernet Controller activity indicator, active low.
20 mA or more current sink capability at VOL of 0.4V max.
20 mA or more current source capability at VOH of 2.4V min.</td>
<td>O 3.3VSB</td><td></td><td></td>
</tr>
<tr>
<td>NBASET0_LINK_MAX#</td>
<td>D97</td>
<td>NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G etc).
20 mA or more current sink capability at VOL of 0.4V max.
20 mA or more current source capability at VOH of 2.4V min.</td>
<td>O 3.3VSB</td><td></td><td></td>
</tr>
<tr>
<td>NBASET0_LINK_MID#</td>
<td>D98</td>
<td>NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.
20 mA or more current sink capability at VOL of 0.4V max.
20 mA or more current source capability at VOH of 2.4V min.</td>
<td>O 3.3VSB</td><td></td><td></td>
</tr>
<tr>
<td>~~NBASET0_CTREF~~</td>
<td>~~C99~~</td>
<td>~~Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.~~</td>
<td>~~REF GND min 3.3V max~~</td><td></td><td>Not supported</td>
</tr>
<tr>
<td>NBASET0_SDP</td>
<td>C98</td>
<td>NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.</td>
<td>IO 3.3VSB</td><td></td><td>Depends on LAN controller SKU</td>
</tr>
</table>

4.3.3 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIe00_TX+ PCIe00_TX- PCIe01_TX+ PCIe01_TX- PCIe02_TX+ PCIe03_TX- PCIe03_TX+ PCIe03_TX- PCIe04_TX+ PCIe04_TX- PCIe05_TX+ PCIe05_TX- PCIe06_TX+ PCIe06_TX- PCIe07_TX+ PCIe07_TX-	D62 D61 D65 D64 D68 D67 D71 D70 D74 D73 D77 D76 D80 D79 D83 D82	PCI Express Differential Transmit Pairs 0-7 PCIe Group 0 Low	O PCIe		AC coupled on Module
PCIe00_RX+ PCIe00_RX- PCIe01_RX+ PCIe01_RX- PCIe02_RX+ PCIe02_RX- PCIe03_RX+ PCIe03_RX- PCIe04_RX+ PCIe04_RX- PCIe05_RX+ PCIe05_RX- PCIe06_RX+ PCIe06_RX- PCIe07_RX+ PCIe07_RX-	C63 C62 C66 C65 C69 C68 C72 C71 C75 C74 C78 C77 C81 C80 C84 C83	PCI Express Differential Receive Pairs 0-7 PCIe Group 0 Low	I PCIe		AC coupled off Module
PCIe08_TX+ PCIe08_TX- PCIe09_TX+ PCIe09_TX-	A63 A62 A66 A65	PCI Express Differential Transmit Pairs 8-15 PCIe Group 0 High A Server Module may map up to 8 higher bandwidth PCIe lanes to Group 0 High	O PCIe		AC coupled on Module

PCIe10_TX+ PCIe10_TX- PCIe11_TX+ PCIe11_TX- PCIe12_TX+ PCIe12_TX- PCIe13_TX+ PCIe13_TX- PCIe14_TX+ PCIe14_TX- PCIe15_TX+ PCIe15_TX-	A69 A68 A72 A71 A75 A74 A78 A77 A81 A80 A84 A83				
PCIe08_RX+ PCIe08_RX- PCIe09_RX+ PCIe09_RX- PCIe10_RX+ PCIe10_RX- PCIe11_RX+ PCIe11_RX- PCIe12_RX+ PCIe12_RX- PCIe13_RX+ PCIe13_RX- PCIe14_RX+ PCIe14_RX- PCIe15_RX+ PCIe15_RX-	B62 B61 B65 B64 B68 B67 B71 B70 B74 B73 B77 B76 B80 B79 B83 B82	PCI Express Differential Receive Pairs 8-15 PCIe Group 0 High A Server Module may map up to 8 higher bandwidth PCIe lanes to Group 0 High	I PCIe		AC coupled off Module
PCIe16_TX+ PCIe16_TX- PCIe17_TX+ PCIe17_TX- PCIe18_TX+ PCIe18_TX- PCIe19_TX+ PCIe19_TX- PCIe20_TX+ PCIe20_TX- PCIe21_TX+	E46 E46 E49 E48 E52 E51 E55 E54 E58 E57 E61	PCI Express Differential Transmit Pairs 16-31 PCIe Group 1	O PCIe		AC coupled on Module

PCIe21_TX- PCIe22_TX+ PCIe22_TX- PCIe23_TX+ PCIe23_TX- PCIe24_TX+ PCIe24_TX- PCIe25_TX+ PCIe25_TX- PCIe26_TX+ PCIe26_TX- PCIe27_TX+ PCIe27_TX- PCIe28_TX+ PCIe28_TX- PCIe29_TX+ PCIe29_TX- PCIe30_TX+ PCIe30_TX- PCIe31_TX+ PCIe31_TX-	E60 E64 E63 E67 E66 H45 H44 H48 H47 H51 H50 H54 H53 H57 H56 H60 H59 H63 H62 H66 H65				
PCIe16_RX+ PCIe16_RX- PCIe17_RX+ PCIe17_RX- PCIe18_RX+ PCIe18_RX- PCIe19_RX+ PCIe19_RX- PCIe20_RX+ PCIe20_RX- PCIe21_RX+ PCIe21_RX- PCIe22_RX+ PCIe22_RX- PCIe23_RX+ PCIe23_RX- PCIe24_RX+ PCIe24_RX-	F45 F44 F48 F47 F51 F50 F54 F53 F57 F56 F60 F59 F63 F62 F66 F65 G46 G45	PCI Express Differential Receive Pairs 16-31 PCIe Group 1	I PCIe		AC coupled off Module

PCIe25_RX+	G49				
PCIe25_RX-	G48				
PCIe26_RX+	G52				
PCIe26_RX-	G51				
PCIe27_RX+	G55				
PCIe27_RX-	G54				
PCIe28_RX+	G58				
PCIe28_RX-	G57				
PCIe29_RX+	G61				
PCIe29_RX-	G60				
PCIe30_RX+	G64				
PCIe30_RX-	G63				
PCIe31_RX+	G67				
PCIe31_RX-	G66				
PCIe32_TX+	E22	PCI Express Differential Transmit Pairs 32-47 PCIe Group 2	O PCIe		AC coupled on Module
PCIe32_TX-	E21				
PCIe33_TX+	E25				
PCIe33_TX-	E24				
PCIe34_TX+	E28				
PCIe34_TX-	E27				
PCIe35_TX+	E31				
PCIe35_TX-	E30				
PCIe36_TX+	E34				
PCIe36_TX-	E33				
PCIe37_TX+	E37				
PCIe37_TX-	E36				
PCIe38_TX+	E40				
PCIe38_TX-	E39				
PCIe39_TX+	E43				
PCIe39_TX-	E42				
PCIe40_TX+	H22				
PCIe40_TX-	H21				
PCIe41_TX+	H24				
PCIe41_TX-	H23				
PCIe42_TX+	H27				
PCIe42_TX-	H26				
PCIe43_TX+	H30				
PCIe43_TX-	H29				
PCIe44_TX+	H33				

PCIe44_TX- PCIe45_TX+ PCIe45_TX- PCIe46_TX+ PCIe46_TX- PCIe47_TX+ PCIe47_TX-	H32 H36 H35 H39 H38 H42 H41				
PCIe32_RX+ PCIe32_RX- PCIe33_RX+ PCIe33_RX- PCIe34_RX+ PCIe34_RX- PCIe35_RX+ PCIe35_RX- PCIe36_RX+ PCIe36_RX- PCIe37_RX+ PCIe37_RX- PCIe38_RX+ PCIe38_RX- PCIe39_RX+ PCIe39_RX- PCIe40_RX+ PCIe40_RX- PCIe41_RX+ PCIe41_RX- PCIe42_RX+ PCIe42_RX- PCIe43_RX+ PCIe43_RX- PCIe44_RX+ PCIe44_RX- PCIe45_RX+ PCIe45_RX- PCIe46_RX+ PCIe46_RX- PCIe47_RX+ PCIe47_RX-	F21 F20 F24 F23 F27 F26 F30 F29 F33 F32 F36 F35 F39 F38 F42 F41 G22 G21 G25 G24 G28 G27 G31 G30 G34 G33 G37 G36 G40 G39 G43 G42	PCI Express Differential Receive Pairs 32-47 PCIe Group 2	I PCIe		AC coupled off Module

~~PCIe48_TX+~~ ~~PCIe48_TX-~~ ~~PCIe49_TX+~~ ~~PCIe49_TX-~~ ~~PCIe50_TX+~~ ~~PCIe50_TX-~~ ~~PCIe51_TX+~~ ~~PCIe51_TX-~~ ~~PCIe52_TX+~~ ~~PCIe52_TX-~~ ~~PCIe53_TX+~~ ~~PCIe53_TX-~~ ~~PCIe54_TX+~~ ~~PCIe54_TX-~~ ~~PCIe55_TX+~~ ~~PCIe55_TX-~~ ~~PCIe56_TX+~~ ~~PCIe56_TX-~~ ~~PCIe57_TX+~~ ~~PCIe57_TX-~~ ~~PCIe58_TX+~~ ~~PCIe58_TX-~~ ~~PCIe59_TX+~~ ~~PCIe59_TX-~~ ~~PCIe60_TX+~~ ~~PCIe60_TX-~~ ~~PCIe61_TX+~~ ~~PCIe61_TX-~~ ~~PCIe62_TX+~~ ~~PCIe62_TX-~~ ~~PCIe63_TX+~~ ~~PCIe63_TX-~~	~~E70~~ ~~E69~~ ~~E73~~ ~~E72~~ ~~E76~~ ~~E75~~ ~~E79~~ ~~E78~~ ~~E82~~ ~~E81~~ ~~E85~~ ~~E84~~ ~~E88~~ ~~E87~~ ~~E91~~ ~~E90~~ ~~H69~~ ~~H68~~ ~~H72~~ ~~H71~~ ~~H75~~ ~~H74~~ ~~H78~~ ~~H77~~ ~~H81~~ ~~H80~~ ~~H84~~ ~~H83~~ ~~H87~~ ~~H86~~ ~~H91~~ ~~H90~~	~~PCI Express Differential Transmit Pairs 48~63~~ ~~PCIe Group 3~~	~~O PCIe~~		Not supported
~~PCIe48_RX+~~ ~~PCIe48_RX-~~ ~~PCIe49_RX+~~ ~~PCIe49_RX-~~ ~~PCIe50_RX+~~ ~~PCIe50_RX-~~ ~~PCIe51_RX+~~	~~F69~~ ~~F68~~ ~~F72~~ ~~F71~~ ~~F75~~ ~~F74~~ ~~F78~~	~~PCI Express Differential Receive Pairs 48~63~~ ~~PCIe Group 3~~	~~I PCIe~~		Not supported

~~PCIe51_RX-~~ ~~PCIe52_RX+~~ ~~PCIe52_RX-~~ ~~PCIe53_RX+~~ ~~PCIe53_RX-~~ ~~PCIe54_RX+~~ ~~PCIe54_RX-~~ ~~PCIe55_RX+~~ ~~PCIe55_RX-~~ ~~PCIe56_RX+~~ ~~PCIe56_RX-~~ ~~PCIe57_RX+~~ ~~PCIe57_RX-~~ ~~PCIe58_RX+~~ ~~PCIe58_RX-~~ ~~PCIe59_RX+~~ ~~PCIe59_RX-~~ ~~PCIe60_RX+~~ ~~PCIe60_RX-~~ ~~PCIe61_RX+~~ ~~PCIe61_RX-~~ ~~PCIe62_RX+~~ ~~PCIe62_RX-~~ ~~PCIe63_RX+~~ ~~PCIe63_RX-~~	~~F77~~ ~~F81~~ ~~F80~~ ~~F84~~ ~~F83~~ ~~F87~~ ~~F86~~ ~~F90~~ ~~F89~~ ~~G70~~ ~~G69~~ ~~G73~~ ~~G72~~ ~~G76~~ ~~G75~~ ~~G79~~ ~~G78~~ ~~G82~~ ~~G81~~ ~~G85~~ ~~G84~~ ~~G88~~ ~~G87~~ ~~G91~~ ~~G90~~				
PCIe_BMC_TX- PCIe_BMC_TX+	A59 A60	PCI Express Differential Transmit Pair for Carrier BMC (Board Management Controller)	O PCIe		AC coupled on Module
PCIe_BMC_RX- PCIe_BMC_RX+	B58 B59	PCI Express Differential Transmit Pair for Carrier BMC (Board Management Controller)	I PCIe		AC coupled off Module
PCIe_REFCLK0_LO- PCIe_REFCLK0_LO+	C59 C60	Reference clock pair for PCIe lanes [0:7], also referred to PCIe Group 0 Low and for the PCIe_BMC link	O PCIe		
PCIe_REFCLK0_HI- PCIe_REFCLK0_HI+	C57 C56	Reference clock pair for PCIe lanes [8:15], also referred to PCIe Group 0 High	O PCIe		
PCIe_REFCLK1- PCIe_REFCLK1+	E93 E94	Reference clock pair for PCIe lanes [16:31], also referred to PCIe Group 1	O PCIe		
PCIe_REFCLK2- PCIe_REFCLK2+	F92 F93	Reference clock pair for PCIe lanes [32:47], also referred to PCIe Group 2	O PCIe		

~~PCIe_REFCLK3-~~ ~~PCIe_REFCLK3+~~	~~G93~~ ~~G94~~	~~Reference clock pair for PCIe lanes [48:63], also referred to PCIe Group 2~~	~~O PCIe~~		Not Supported
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signals from Carrier devices for PCIe_REFCLK0_LO clock pair	I/O OD 3.3V	PU 10K 3.3V	
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signals from Carrier devices for PCIe_REFCLK0_HI clock pair	I/O OD 3.3V	PU 10K 3.3V	
PCIe_CLKREQ0_1#	E96	PCIe reference clock request signals from Carrier devices for PCIe_REFCLK1 clock pair	I/O OD 3.3V	PU 10K 3.3V	
PCIe_CLKREQ0_2#	E97	PCIe reference clock request signals from Carrier devices for PCIe_REFCLK2 clock pair	I/O OD 3.3V	PU 10K 3.3	
~~PCIe_CLKREQ0_3#~~	~~F95~~	~~PCIe reference clock request signals from Carrier devices for PCIe_REFCLK3 clock pair~~	~~I/O OD 3.3V~~	~~PU 10K 3.3V~~	Not supported

4.3.4 USB

To realize a COM-HPC USB 3.2 Gen1, ~~Gen2, Gen2x2 or USB4~~ port, one of the four available USB 2.0 ports from the USB[0:3] pool must be used along with the SuperSpeed pins. Specific pairings are described in table below.

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0- USB1+ USB1- USB2+ USB2- USB3+ USB3-	D17 D16 D14 D13 C18 C17 C15 C14	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports. If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool.	I/O 3.3VSB		USB 1.1/2.0 compliant USB Client mode – Not supported
~~USB4+~~ ~~USB4-~~ ~~USB5+~~ ~~USB5-~~ ~~USB6+~~ ~~USB6-~~	~~B17~~ ~~B16~~ ~~B14~~ ~~B13~~ ~~A18~~ ~~A17~~	~~USB 2.0 differential pairs, channels 0 through 7.~~ ~~USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.~~	~~I/O 3.3VSB~~		Not supported

~~USB7+~~ ~~USB7-~~	~~A15~~ ~~A14~~	~~If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool.~~			
USB0_SSTX0+ USB0_SSTX0- USB1_SSTX0+ USB1_SSTX0- ~~USB0_SSTX1+~~ ~~USB0_SSTX1-~~ ~~USB1_SSTX1+~~ ~~USB1_SSTX1-~~	D44 D43 D38 D37 ~~D47~~ ~~D46~~ ~~D41~~ ~~D40~~	Four sets of SuperSpeed transmit pairs, used to realize the transmit side of two USB 3.2 Gen 2x2 ports. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair and so on, USB1_SSxxx+/- with the USB1 USB 2.0 pair).	O PCIe		AC coupled on Module
USB0_SSRX0+ USB0_SSRX0- USB1_SSRX0+ USB1_SSRX0- ~~USB0_SSRX1+~~ ~~USB0_SSRX1-~~ ~~USB1_SSRX1+~~ ~~USB1_SSRX1-~~	C45 C44 C39 C38 ~~C48~~ ~~C47~~ ~~C42~~ ~~C41~~	Four sets of SuperSpeed receive pairs, used to realize the transmit side of two USB 3.2 Gen 2x2 ports. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair and so on, USB1_SSxxx+/- with the USB1 USB 2.0 pair).	I PCIe		AC coupled off Module
USB2_SSTX+ USB2_SSTX- USB3_SSTX+ USB3_SSTX-	D35 D34 D32 D31	Two sets of high speed transmit pairs, to realize two USB 3.2 Gen 1 or Gen 2 implementations. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2_SSxxx+/- shall be used with the USB2 USB 2.0 pair and USB3_SSxxx+/- with the USB3 USB 2.0 pair).	O PCIe		AC coupled on Module
USB2_SSRX+ USB2_SSRX- USB3_SSRX+ USB3_SSRX-	C36 C35 C33 C32	Two sets of high speed receive pairs, to realize two USB 3.2 Gen 1 or Gen 2 implementations. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2_SSxxx+/-	I PCIe		AC coupled off Module

		shall be used with the USB2 USB 2.0 pair and USB3_SSxxx+/- with the USB3 USB 2.0 pair).			
USB01_OC# USB23_OC# ~~USB45_OC#~~ ~~USB67_OC#~~	B28 B27 ~~B26~~ ~~B25~~	USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the Module. The pull-up should be 10K. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not pull these lines up. Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item.	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
RSMRST_OUT#		USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state. RSMRST_OUT# is also described in Power and System Management section	O 3.3VSB	PD 1K	

This platform doesn't support USB4, thus additional signals required by USB4 are not shown here.

4.3.5 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	D53 D52	Serial ATA Channel 0 transmit differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	D50 D49	Serial ATA Channel 0 receive differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	D59 D58	Serial ATA Channel 1 transmit differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	D56 D55	Serial ATA Channel 1 receive differential pair.	I SATA		AC coupled on Module

4.3.6 Asynchronous Serial Port

Name	Pin #	Description	I/O	PU / PD	Comment
UART0_TX UART1_TX	C89 B87	Logic level asynchronous serial port transmit signal	O 3.3V		
UART0_RX UART1_RX	C90 B88	Logic level asynchronous serial port receive signal	I 3.3V	PU 10K 3.3V	
UART0_RTS# ~~UART1_RTS#~~	C91 ~~B89~~	Logic level asynchronous serial port Request to Send signal, active low	O 3.3V		UART1_RTS# Not supported
UART0_CTS# ~~UART1_CTS#~~	C92 ~~B90~~	Logic level asynchronous serial port Clear to Send input, active low	I 3.3V		UART1_CTS# Not supported

4.3.7 I2C

Two general purpose I2C ports are defined for COM-HPC. The first of the two supports an ALERT# input. I2C0 is defined to operate from a 3.3V rail and I2C1 from a 1.8V rail.

Name	Pin #	Description	I/O	PU / PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 3.3VSB	PU 4.7K 3.3VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 3.3VSB	PU 4.7K 3.3VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 3.3V	PU 10K 3.3VSB	
I2C1_CLK	C96	Clock I/O line for the general purpose I2C1 port	I/O OD 1.8VSB	PU 4.7K 1.8VSB	
I2C1_DAT	C97	Data I/O line for the general purpose I2C1 port	I/O OD 1.8VSB	PU 4.7K 1.8VSB	

4.3.8 eSPI

Name	Pin #	Description	I/O	PU / PD	Comment
eSPI_IO0 eSPI_IO1 eSPI_IO2 eSPI_IO3	A50 A51 A52 A53	eSPI Master Data Input / Outputs. These are bi directional input/output pins used to transfer data between master and slaves.	I/O CMOS 1.8VSB	PU 10K 1.8VSB	
eSPI_CS0# eSPI_CS1#	B54 B55	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.	O COMS 1.8VSB	PU 10K 1.8VSB	
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations.	O CMOS 1.8VSB		
eSPI_ALERT0# eSPI_ALERT1#	B52 B53	eSPI pins used by eSPI slave to request service from the eSPI master.	I COMS 1.8VSB	PU 10K 1.8VSB	
ESPI_RST#	B56	eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves.	O CMOS 1.8VSB		

4.3.9 Boot SPI (BIOS ONLY) and Boot Select

Name	Pin #	Description	I/O	PU / PD	Comment
BOOT_SPI_CS#	B48	Chip select for Carrier Board SPI. See Table 20 "BIOS Select Options: Module eSPI and SPI Chip Select Routing" for implementation details. If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 10K	
BOOT_SPI_IO0 BOOT_SPI_IO1 ~~BOOT_SPI_IO2~~ ~~BOOT_SPI_IO3~~	C50 C51 ~~C52~~ ~~C53~~	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI	I/O CMOS VCC_BOOT_SPI		BOOT_SPI_IO2 and BOOT_SPI_IO3: Not Supported

		in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)			
BOOT_SPI_CLK	C54	Clock from Module chipset to Carrier SPI	O VCC_BOOT_SPI		Clock support is 48MHz, can be adjusted by project basis
VCC_BOOT_SPI	B47	Power supply for Carrier Board SPI – sourced from Module – nominally either 1.8V or 3.3V. The Module shall provide a minimum of 100mA on VCC_BOOT_SPI. Carriers shall use less than 100mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the Carrier Board. The Module vendor may choose what power domains the BOOT_SPI is active in.	O 3.3VSB		
BSEL2 BSEL1 BSEL0	B51 B50 B49	Boot Select pins. These pins distinguish between a SPI or eSPI BIOS boot and between an on—Module or off-Module BIOS. Details are in Table 20: BIOS Select Options: Module eSPI and SPI Chip Select Routing. Pulled up on Module to vendor specific power rail	I	PU 10K	

4.3.10 Port 80 Support on USB_PD I2C Bus

COM-HPC Module should support exporting Port 80 information over the USB_PD I2C bus (signals USB_PD_I2C_DAT and USB_PD_I2C_CLK) (pin B36 and B35) to Carrier hardware that implements a pair of 7-segment displays to show the codes.

Name	Pin #	Description	I/O	PU / PD	Comment
USB_PD_I2C_DAT	B36	I2C data line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	OD 3.3VB	PU 4K7 3.3VSB	
USB_PD_I2C_CLK	B35	I2C clock line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	OD 3.3VSB	PU 4K7 3.3VSB	
~~USB_PD_ALERT#~~	~~B34~~	~~I2C clock line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.~~	~~I~~ ~~3.3VSB~~		Not Supported

4.3.11 IPMB

The IPMB (Intelligent Platform Management Bus) is used (optionally) with a Carrier based BMC (Board Management Controller) Master. On the module, the IPMB should be routed to and used with an MMC (Module Management Controller). The Module IPMB is a slave port.

Name	Pin #	Description	I/O	PU / PD	Comment
IPMB_CLK	B91	Clock I/O line for the multi-master IPMB port	I/O OD CMOS 3.3VB	PU 47K 3.3VSB	
IPMB_DAT	B92	Data I/O line for the multi-master IPMB port	I/O OD CMOS 3.3VSB	PU 47K 3.3VSB	

4.3.12 General Purpose SPI

Name	Pin #	Description	I/O	PU / PD	Comment
~~GP_SPI_MISO~~	~~B94~~	~~Serial data into the COM-HPC Module from the Carrier GP_SPI device ("Master In Slave Out")~~	~~I 3.3V~~	~~PU 10K~~	Not supported
~~GP_SPI_MOSI~~	~~B93~~	~~Serial data from the COM-HPC Module to the Carrier GP_SPI device ("Master Out Slave In")~~	~~O 3.3V~~		Not supported
~~GP_SPI_CLK~~	~~B99~~	~~Clock from the Module to Carrier GP_SPI device~~	~~O 3.3V~~		Not supported
~~GP_SPI_CS0#~~ ~~GP_SPI_CS1#~~ ~~GP_SPI_CS2#~~ ~~GP_SPI_CS3#~~	~~B95~~ ~~B96~~ ~~B97~~ ~~B98~~	~~GP_SPI chip selects, active low~~	~~O 3.3V~~		Not supported
~~GP_SPI_ALERT#~~	~~B100~~	~~Alert (interrupt) from a Carrier GP_SPI device to the Module~~	~~I 3.3V~~	~~PU 10K~~	Not supported

4.3.13 Power & System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	I 3.3VSB	PU 4K7 3.3VSB	
RSTBTN#	C02	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle ***may*** be used.	I 3.3VSB	PU 10K 3.3VSB	
PLTRST#	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and ***may*** result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or ***may*** be initiated by the Module software..	O 3.3VSB		
VIN_PWR_OK	C06	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.	I 3.3V	PU 10K 3.3VSB	
SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board ***should*** be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.	O 3.3VSB		
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3VSB		
SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	O 3.3VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 3.3VSB	PU 10K 3.3VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	
BATLOW#	A11	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly	I 3.3VSB	PU 10K 3.3VSB	

		transitioning to power saving or power cut-off ACPI modes.			
~~TAMPER#~~	~~B06~~	~~Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.~~			Not Supported
RSMRST_OUT#	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.	O 3.3VSB		

4.3.14 Rapid Shutdown

Name	Pin #	Description	I/O	PU / PD	Comment
~~RAPID_SHUTDOWN~~	~~E1~~	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.~~	~~I 5VSB~~		Not supported

4.3.15 Thermal Protection

Name	Pin #	Description	I/O	PU / PD	Comment
CARRIER_HOT#	C04	Input from off-Module temp sensor indicating an over-temp situation.	I 3.3V	PU 100K 3.3V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 4.99K 3.3V	

4.3.16 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 3.3VSB	PU 4.7K 3.3VSB	The maximum capacitance on the Carrier Board shall not exceed 100pF
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU 4.7K 3.3VSB	The maximum capacitance on the Carrier Board shall not exceed 100Pf
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3VSB	PU 4.7K 3.3VSB	The maximum capacitance on the Carrier Board shall not exceed 100pF

4.3.17 General Purpose Input Outputs

Name	Pin #	Description	I/O	PU / PD	Comment
GPIO_00 GPIO_01 GPIO_02 GPIO_03 GPIO_04 GPIO_05 GPIO_06 GPIO_07 GPIO_08 GPIO_09 GPIO_10 GPIO_11	A88 A89 A90 A91 A92 A93 A94 A95 A96 A97 A98 A99	General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the Module host.	I/O 3.3V	PU 100K 3.3V	

4.3.18 Module Type Definition

<table>
<tr><th>Name</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0
TYPE1
TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5V or less. Carrier hardware reads the level on these straps.

<table>
<tr><th></th><th colspan="3">Module Connections</th><th>Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th><th></th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server Module – Fixed 12V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client Module - Wide Range 8V to 20V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client Module – Fixed 12V input</td></tr>
</table>

The Module shall implement all three TYPE[x] pins per the table above.

The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM-HPC Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED.</td><td></td><td>Server Module – Fixed 12V input</td></tr>
</table>

4.3.19 Miscellaneous Signals

Name	Pin #	Description	I/O	PU / PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred. Refer to Section 5.3 for details.	O 3.3V		
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 3.3V	PU 100K 3.3V	
FAN_PWMOUT	C11	Fan speed control for a secondary system fan. The primary fan control signals for CPU thermal management are on the Module, along with a vendor specific connector. Fan controls use the Pulse Width Modulation (PWM) technique to control the fan's RPM. CMOS output; Carrier designers should buffer this signal with an open drain FET and pullup or other robust Carrier device(s).	O 3.3V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse output for the secondary fan.	I OD 3.3V	PU 10K 3.3V	
RSVD		Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.			

4.3.20 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC	A01-A09 B01 B03 B05 B07 B09 C01 C03 C05 C07 C09 D01-D09	Primary power input: fixed +12V on the Client Type 0; wide range +8V to +20V on the Client Type 1; fixed +12V on the Server. All available VCC pins on the connector shall be used.	P		12V +/- 5%
~~VCC_5V_SBY~~	~~B24~~	~~Standby power input: +5.0V nominal.~~ ~~Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.~~	~~P~~		Not Supported
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND		Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane(s).	P		

5. Additional Features

This chapter describes the connectors, LEDs, and switches, located on the module and are not necessarily included in the PICMG standard specification. The locations of these parts are as shown below:

XDP debug header (Chris)

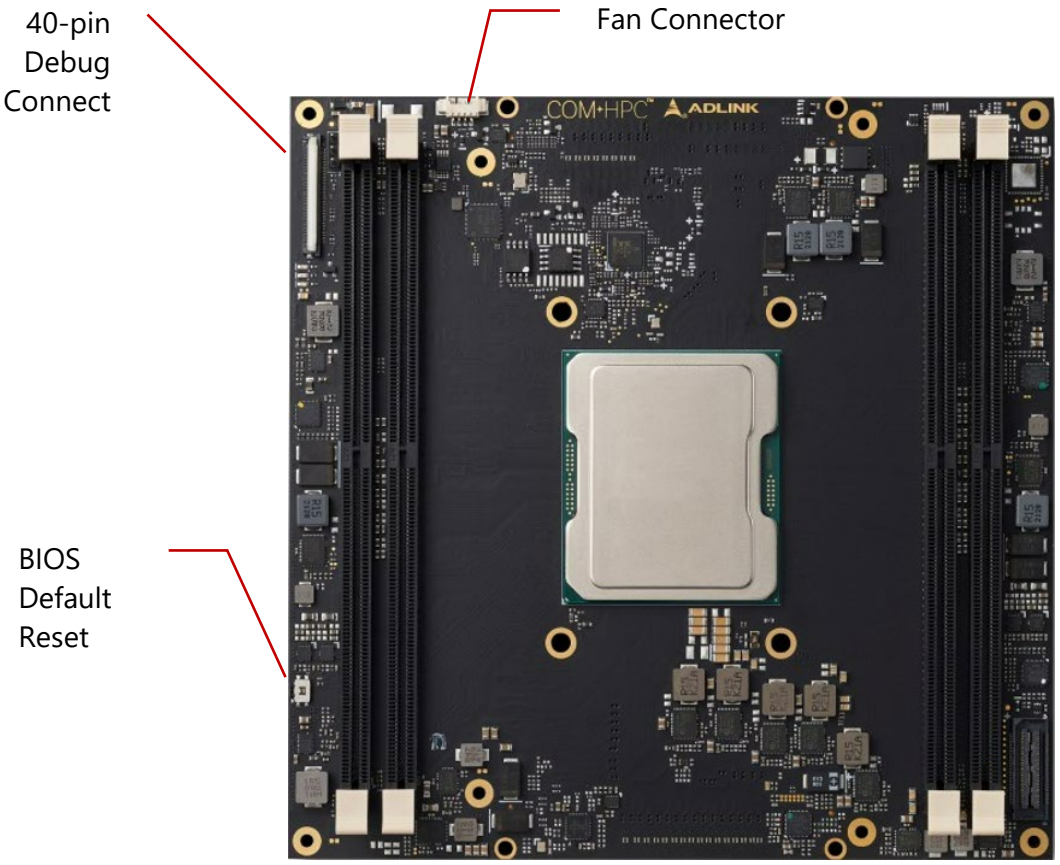


Figure 3 – Module feature locations (front)

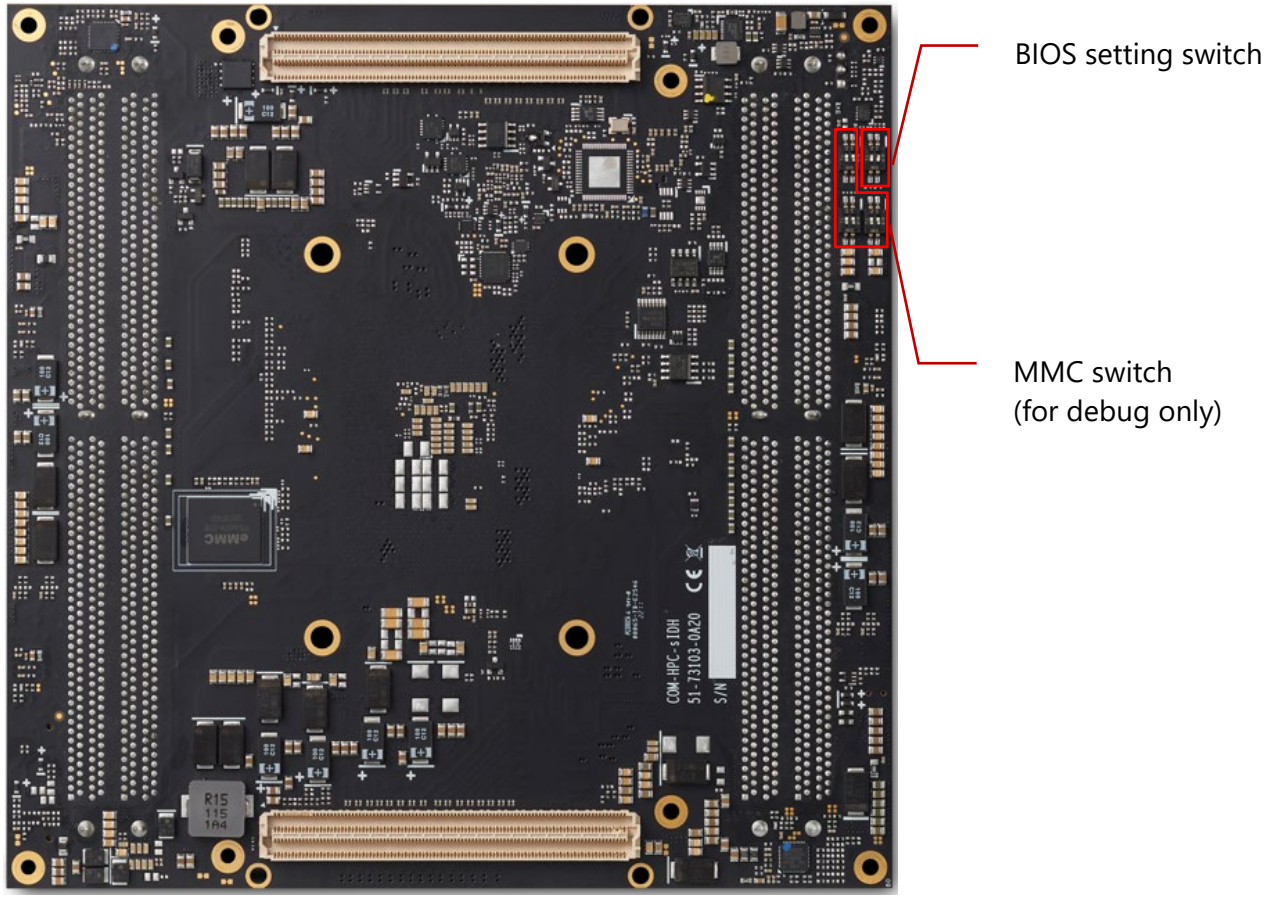


Figure 4 – Module feature locations (bottom)

5.1 Debug Connector (40-pin connector)

This connector is particular useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points for measurement of internal power rails
- SPI BIOS programming interface
- I2C bus for BIOS POST code readout
- Module EC and MMC programming interface

5.2 Status LEDs

Status LEDs are mounted on the module as below

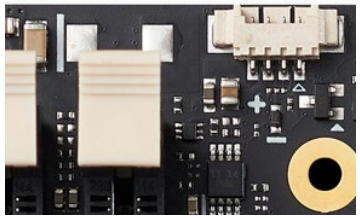
Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, Reset (see Exception Codes Table below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a Reset not initiated by the BMC can clear the WD LED (user action)

5.3 Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD
24	NO_PCH_PG

5.4 Fan Connector

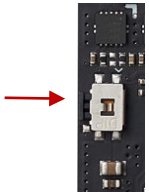
Connector Type: JVE 24W1125A-04M00



Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V*

The supply voltage and maximum current of the fan connector is dependent on the module's input voltage (VCC_12V pins)

5.5 BIOS Default Reset



To perform a hardware reset of the default BIOS settings, follow the steps below:

1. Shut down the system.
2. Hold down the BIOS Setup Defaults Reset Button continuously and boot up the system. You can release the button when the BIOS prompt screen appears.
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.

5.6 BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch, Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default, TBC)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

5.7 MIPI 60 Debug Header

The MIPI60 debug header is a connection into a target-system environment that provides access to JTAG, run control, system control, and observation resources.

Pin	MIPI60 Signal	Pin	MIPI60 Signal
1	VREF_DEBUG	2	TMS/TMSC
3	TCK	4	TDO/EXTA
5	TDI/EXTB	6	nRESET
7	RTCK/EXTC	8	TRST_PD
9	nTRST/EXTD	10	EXTE/TRIGIN
11	EXTF/TRIGOUT	12	VERF_TRACE
13	TRC_CLK[0]	14	TRC_CLK[1]
15	Target Presence Detection	16	GND
17	TRC_DATA[0][0]	18	TRC_DATA1[0] / TRC_DATA0[10]
19	TRC_DATA[0][1]	20	TRC_DATA1[1] / TRC_DATA0[21]
21	TRC_DATA[0][2]	22	TRC_DATA1[2] / TRC_DATA0[22]
23	TRC_DATA[0][3]	24	TRC_DATA1[3] / TRC_DATA0[23]
25	TRC_DATA[0][4]	26	TRC_DATA1[4] / TRC_DATA0[24]
27	TRC_DATA[0][5]	28	TRC_DATA1[5] / TRC_DATA0[25]
29	TRC_DATA[0][6]	30	TRC_DATA1[6] / TRC_DATA0[26]
31	TRC_DATA[0][7]	32	TRC_DATA1[7] / TRC_DATA0[27]
33	TRC_DATA[0][8]	34	TRC_DATA1[8] / TRC_DATA0[28]
35	TRC_DATA[0][9]	36	TRC_DATA1[9] / TRC_DATA0[29]
37	TRC_DATA3[0] / TRC_DATA0[10]	38	TRC_DATA2[0] / TRC_DATA1[10] / TRC_DATA0[30]

Pin	MIPI60 Signal	Pin	MIPI60 Signal
39	TRC_DATA3[1] / TRC_DATA0[11]	40	TRC_DATA2[1] / TRC_DATA1[11] / TRC_DATA0[31]
41	TRC_DATA3[2] / TRC_DATA0[12]	42	TRC_DATA2[2] / TRC_DATA1[12] / TRC_DATA0[32]
43	TRC_DATA3[3] / TRC_DATA0[13]	44	TRC_DATA2[3] / TRC_DATA1[13] / TRC_DATA0[33]
45	TRC_DATA3[4] / TRC_DATA0[14]	46	TRC_DATA2[4] / TRC_DATA1[14] / TRC_DATA0[34]
47	TRC_DATA3[5] / TRC_DATA0[15]	48	TRC_DATA2[5] / TRC_DATA1[15] / TRC_DATA0[35]
49	TRC_DATA3[6] / TRC_DATA0[16]	50	TRC_DATA2[6] / TRC_DATA1[16] / TRC_DATA0[36]
51	TRC_DATA3[7] / TRC_DATA0[17]	52	TRC_DATA2[7] / TRC_DATA1[17] / TRC_DATA0[37]
53	TRC_DATA3[8] / TRC_DATA0[18]	54	TRC_DATA2[8] / TRC_DATA1[18] / TRC_DATA0[38]
55	TRC_DATA3[9] / TRC_DATA0[19]	56	TRC_DATA2[9] / TRC_DATA1[19] / TRC_DATA0[39]
57	Connect to GND plane	58	GND
59	TRC_CLK[3]	60	TRC_CLK[2]

6. System Resources

6.1 System Memory Map

Address Range (hex)	Description
23000000000-23FFFFFFFF	PCI Express Root Complex
22000000000-22FFFFFFFF	PCI Express Root Complex
22FB8000000-22FFC4FFFF	PCI Express Root Complex
21000000000-21FFFFFFFF	PCI Express Root Complex
20000000000-20FFFFFFFF	PCI Express Root Complex
20FFFA99000-20FFFA99FFF	CDF ME: HECI#1 – 18D3
20FFFA98000-20FFFA98FFF	CDF ME: HECI#3 – 18D6
20FFFA97000-20FFFA97FFF	SDA Standard Compliant SD Host Controller
20FFFA96000-20FFFA96FFF	Intel USB 3.0 eXtensible Host Controller
20FFFA20000-20FFFA3FFF	CDF PCIeRP[8]-18AD
20FFFA00000-20FFFA1FFF	CDF PCIeRP[9]-18AE
FF000000-FFFFFFFF	Motherboard resource
FED00000-FED003FF	Hight precision event timer
FEC00000-FECFFFFF	Advance programmable interrupt controller
FE200000-FE7FFFFF	Motherboard resources
FE000000-FE01FFFF	Motherboard resources
FD6F0000-FDFFFFFF	Motherboard resources
FD000000-FD69FFFF	Motherboard resources
E1000000-FB7FFFFF	PCI Express Root Complex
C6000000-E0FFFFFF	PCI Express Root Complex

Address Range (hex)	Description
AB000000-C5FFFFFF	PCI Express Root Complex
90000000-AAFFFFFF	PCI Express Root Complex
000C8000-000CFFFF	PCI Express Root Complex
000A0000-000BFFFF	PCI Express Root Complex

6.2 I/O Map

Hex Range	Device
00h - 0Fh	DMA controller
00h – CF7h	PCI Express Root Complex
10h - 1Fh	Motherboard resources
20h – 3Dh	Programmable interrupt controller
2Eh - 2Fh 4Eh - 4Fh	LPC SIO (IT5121E/AST2500SEC) configuration index/data registers
40h - 43h	System Timer
50h - 53h	System Timer
62h and 66h	ACPI-Compliant Embedded Controller
70h - 77h	Real Time Clock Controller
81h - 83h, 87h, 89h - 8Bh and8Fh	DMA controller
90h - 9Fh	Motherboard resources
A0h - BDh	Programmable interrupt controller
C0h – DFh	Direct memory asscess controller
F0h	Numeric data processor
262h – 263h	Generic IPMI Compliant Device
2F8h – 2FFh	Serial port 2 (COM4)
3B0h – 3BBh	CDF PCIeRP[9]-18AE
3C0h – 3CFh	CDF PCIeRP[9]-18AE
3F8h - 3FFh	Serial port 1 (COM1)
400h - 41Fh	Motherboard resources
4D0h – 4D1h	Programmable interrupt controller

Hex Range	Device
500h – A6Fh	Motherboard resources
1000h – 5FFFh	PCI Express Root Complex
4000h – 407Fh	Microsoft Basic display Complex
5020h – 503Fh 5070h – 5073h 5080h – 5087h	SATA AHCI Controller
6000h – 9FFFh	PCI Express Root Complex
A000h - CFFFh	PCI Express Root Complex
D000h - FFFFh	PCI Express Root Complex

6.3 Interrupt Request (IRQ) Lines

IRQ#	Typical Intterupt Resource	Connected to Pin	Available
0	High precision even timer/System timer		No
3	Serial Port 4		No
4	Serial Port 1		No
8	System CMOS/Real time clock		No
11	CDF ME:HECI		No
13	Numeric data processor		No

6.4 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	Internal	Mesh2IIO MMAP/VT-D
00h	00h	01h	Internal	Mesh2IIO PMON
00h	00h	02h	Internal	Mesh2IIO RAS
00h	00h	03h	Internal	Mesh2IIO DFX
00h	00h	04h	Internal	Satellite IEH
00h	00h	05h	Internal	VMD
00h	01h	00h	Internal	CBDMA CH0
00h	01h	01h	Internal	CBDMA CH1
00h	01h	02h	Internal	CBDMA CH2
00h	01h	03h	Internal	CBDMA CH3
00h	01h	04h	Internal	CBDMA CH4
00h	01h	05h	Internal	CBDMA CH5
00h	01h	06h	Internal	CBDMA CH6
00h	01h	07h	Internal	CBDMA CH7
00h	02h	00h	Internal	PECI Out-Of-Band Management Services Module (OOB-MSM)
00h	02h	01h	Internal	PECI OOB-MSM - Performance Monitoring Unit (PMU)
00h	02h	02h	Internal	Reserved
00h	02h	04h	Internal	CPU Intel® Trace Hub
00h	06h	00h	Internal	Virtual Root Port (VRP) for Intel QAT v1.7
00h	00h	PF: 0 VF: 0-15	Internal	Intel QAT v1.7 (Bus subordinate to S0 VRPis assigned by BIOS)

Bus Number	Device Number	Function Number	Routing	Description
00h	0Eh	00h	Internal	SATA Controller 2
00h	0Fh	00h	Internal	Host SMBUS
00h	14h	00h	Internal	PCH PCIe Cluster 2 Root Port 8
00h	15h	00h	Internal	PCH PCIe Cluster 2 Root Port 9
00h	18h	00h	Internal	Intel® ME – HECI 1
00h	18h	04h	Internal	Intel® ME – HECI 3
00h	1Ah	00h	Internal	HSUART 0
00h	1Ah	01h	Internal	HSUART 1
00h	1Ah	02h	Internal	HSUART 2
00h	1Ah	03h	Internal	Reserved
00h	1Ch	00h	Internal	eMMC Controller
00h	1Dh	00h	Internal	Host Bridge
00h	1Eh	00h	Internal	USB xHCI Controller
00h	1Fh	00h	Internal	LPC/eSPI Controller
00h	1Fh	04h	Internal	Legacy SMBUS
00h	1Fh	05h	Internal	SPI Controller
00h	1Fh	07h	Internal	PCH Intel® Trace Hub
01h	00h	00h	Internal	Intel Ethernet controller
02h	00h	00h	Internal	PCI Bridge
03h	00h	00h	External	AST2500
15h	00h	00h	Internal	Mesh2IIO MMAP/VT-D
15h	00h	01h	Internal	Mesh2IIO PMON
15h	00h	02h	Internal	Mesh2IIO RAS
15h	00h	03h	Internal	Mesh2IIO DFX
84h	00h	00h	Internal	Mesh2IIO MMAP/VT-D

Bus Number	Device Number	Function Number	Routing	Description
84h	00h	01h	Internal	Mesh2IIO PMON
84h	00h	02h	Internal	Mesh2IIO RAS
84h	00h	03h	Internal	Mesh2IIO DFX
84h	00h	04h	Internal	Host Bridge
84	04h	00h	Internal	Virtual Root Port for Network Interface and Scheduler
85h	00h	00h	Internal	Intel Ethernet Controller
85h	00h	01h	Internal	Intel Ethernet Controller
85h	00h	02h	Internal	Intel Ethernet Controller
85h	00h	03h	Internal	Intel Ethernet Controller
85h	00h	04h	Internal	Intel Ethernet Controller
85h	00h	05h	Internal	Intel Ethernet Controller
85h	00h	06h	Internal	Intel Ethernet Controller
85h	00h	07h	Internal	Intel Ethernet Controller
8Ch	00h	00h	Internal	Mesh2IIO MMAP/VT-D
8Ch	00h	01h	Internal	Mesh2IIO PMON
8Ch	00h	02h	Internal	Mesh2IIO RAS
8Ch	00h	03h	Internal	Mesh2IIO DFX
8Ch	00h	04h	Internal	Satellite IEH
FEh	00h	00h	Internal	UBOX - Global Events
FEh	00h	01h	Internal	UBOX
FEh	00h	02h	Internal	UBOX -DEC

Bus Number	Device Number	Function Number	Routing	Description
FEh	00h	03h	Internal	UBOX - Global IEH
FEh	00h	05h	Internal	MS2UBOX
FEh	0Bh	00h	Internal	SPD0_SMBUS
FEh	0Bh	01h	Internal	SPD1_SMBUS
FEh	0Bh	02h	Internal	VPP_SMBUS
FEh	0Ch	00h	Internal	Mesh2IMC0
FEh	0Dh	00h	Internal	Mesh2IMC0
FEh	1Ah	00h	Internal	IMC0
FEh	1Bh	00h	Internal	IMC0
FFh	00h	00h	Internal	CHA0_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	01h	Internal	CHA1_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	02h	Internal	CHA2_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	03h	Internal	CHA3_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	04h	Internal	CHA4_GRP1 - UNICAST_GROUP1_CHA
FFh	00h	05h	Internal	CHA5_GRP1 - UNICAST_GROUP1_CHA
FFh	0Ah	00h	Internal	CHA0_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	01h	Internal	CHA1_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	02h	Internal	CHA2_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	03h	Internal	CHA3_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	04h	Internal	CHA4_GRP0 - UNICAST_GROUP0_CHA
FFh	0Ah	05h	Internal	CHA5_GRP0 - UNICAST_GROUP0_CHA
FFh	1Dh	00h	Internal	CHAALL0 - Multicast DRAM Rules
FFh	1Dh	01h	Internal	CHAALL1 - Multicast MMIO Rules
FFh	1Eh	00h	Internal	PCU
FFh	1Eh	01h	Internal	PCU

Bus Number	Device Number	Function Number	Routing	Description
FFh	1Eh	02h	Internal	PCU
FFh	1Eh	03h	Internal	PCU
FFh	1Eh	04h	Internal	PCU
FFh	1Eh	05h	Internal	PCU
FFh	1Eh	06h	Internal	PCU
FFh	1Eh	07h	Internal	PCU

6.5 PCI Interrupt Routing Map

INT Line	PCI Express Port 0	Crystal Beach DMA Engine0	Lpc Bridge	HECI #1 on PCH	SMBus con-troller on PCH	SATA Controller
Int0	INTA:16	INTA:16		INTA:16		INTA:16
Int1	INTB:17				INTB:17	
Int2	INTC:18		INTC:18			
Int3	INTC:19					

INT Line	XHCI Controller	Intel I210			
Int0	INTA:16	INTA:16			
Int1					
Int2					
Int3					

INT Line	PCIE Port1	PCIE Port 2	PCIE Port 3	PCIE Port 4	PCIE Port 5	PCIE Port 6	PCIE Port 7	PCIE Port 8
Int0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Int1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Int2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Int3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

6.6 SMBus Address Table

Device	Address
DDR4 Channel A(SO-DIMM1)	A0h
DDR4 Channel B(SO-DIMM2)	A2h
DDR4 Channel C(SO-DIMM3)	A4h
DDR4 Channel D(SO-DIMM4)	A6h
Thermal Sensor	90h
Thermal Sensor	92h

7. BIOS Setup

7.1 Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in bold, and the function of each setting is described in the right hand column of the respective table

► indicates a submenu

Main	Platform Configuration	Advanced	Socket Configuration	Server Mgmt	Security
BIOS Information System Information Board Information ► System Date System Time	PCH-IO Configuration► Miscellaneous Config-uration► Network Configuration► Server ME Configuration► iRC Firmware Infor-mation► System Event Log► Reserve Memory►	Serial Port Console Redirection ► PCI Subsystem Settings ► Power Management ► System Management ► Thermal Management ► Watchdog Timer ► Super IO Configuration ► Miscellaneous ► Network Stack Config-uration ► Trusted Computing ►	Processor Configuration► Common RefCode Configura-tion► Uncore Configuration► Memory Configura-tion► IIO Configuration► Advanced Power Manage-mentConfiguration►	BMC Support IPMI Interface TypeWait for BMC FRB-2 Timer FRB-2 Timer timeoutFRB-2 Timer Policy OS Watchdog Timer Serial Mux System Event Log► Bmc self test log► BMC network configuration► View System EventLog► BMC User Settings► BMC warm reset	Password Descrip-tion Secure BootMenu

Boot	Save & Exit
Boot Config- uration	Save Options Default Options Boot Override

8.

8. BIOS Checkpoints, Beep Codes

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to a following initialization step. Error codes signify error conditions encountered in the process of system initialization. The Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but the Aptio 5.x core can be configured to send checkpoints to a variety of sources. The Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. A beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not the only sounds generated during the boot process. Some firmware components may use sounds to notify the user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes

Viewing Checkpoints

Checkpoints generated by the Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-on cards show the value of I/O port 80h on an LED display.

Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

9. Software Support

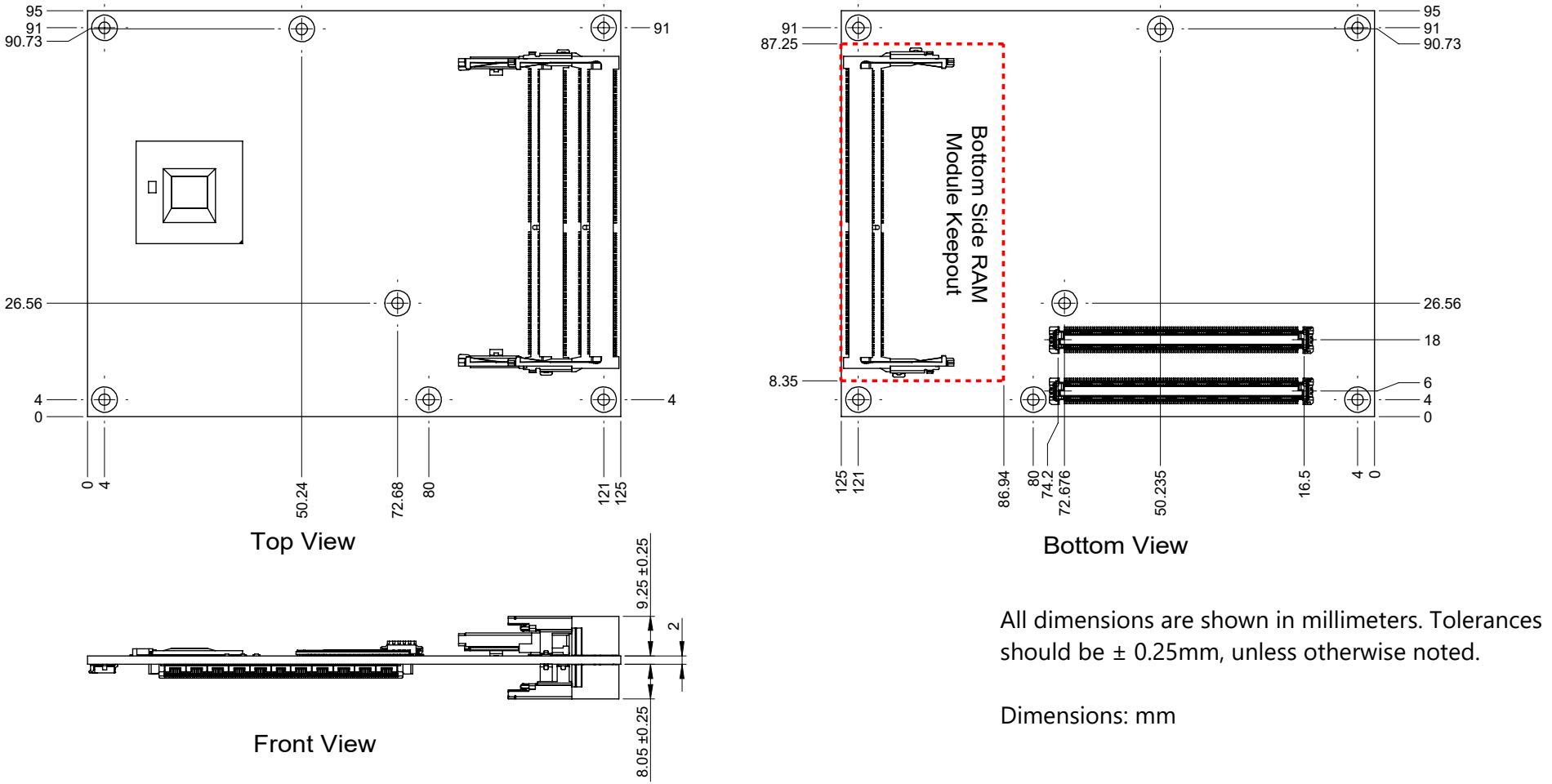
9.1. Windows Server 2019 64-bit

9.2. Windows 10 IoT Enterprise 64-bit

9.3. Yocto Linux 64-bit (TBC)

https://github.com/ADLINK/meta-adlink-x86-64bit (TBC)

10. Mechanical



All dimensions are shown in millimeters. Tolerances should be ± 0.25mm, unless otherwise noted.

Dimensions: mm

Figure 5 – Module mechanical dimensions

11. Thermal

11.1. Thermal Solutions

11.1.1 Heatspreader: HTS

Dimensions: mm

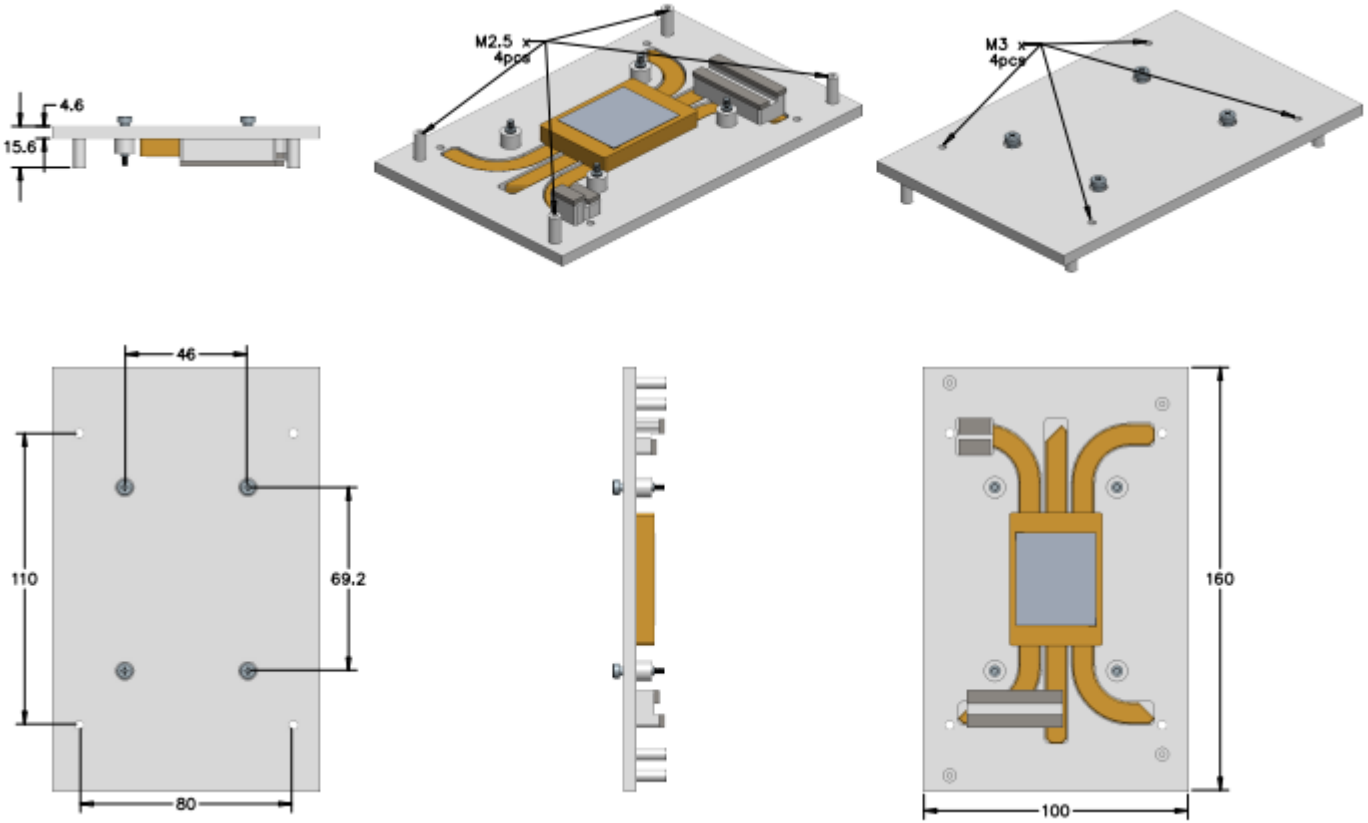


Figure 6 – Heatspreader: HTS

11.1.2 Heatsink: THS-BL

Dimensions: mm

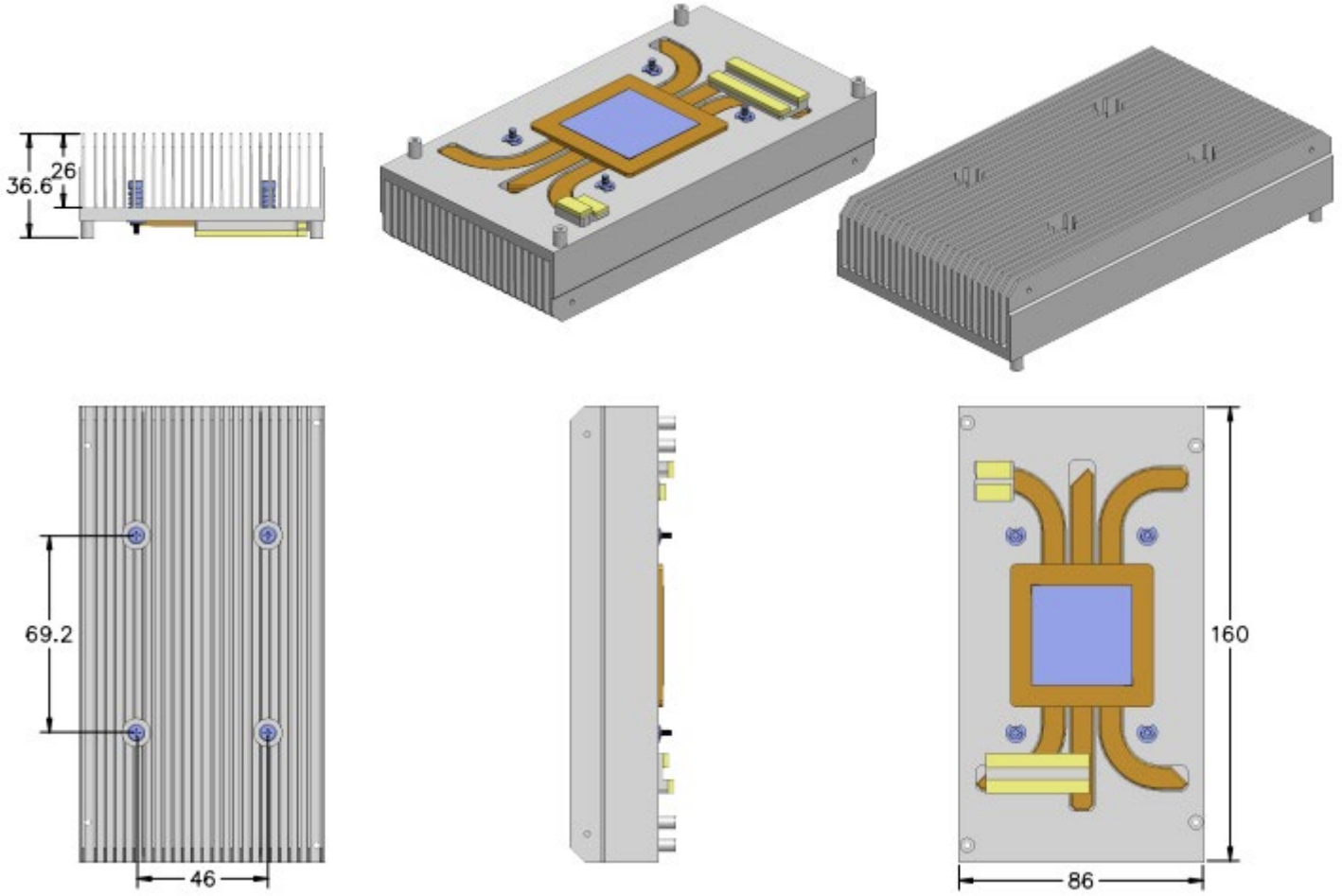


Figure 7 – Heatsink: THS-BL

11.1.3 Heatsink with Fan: THSF

Dimensions: mm

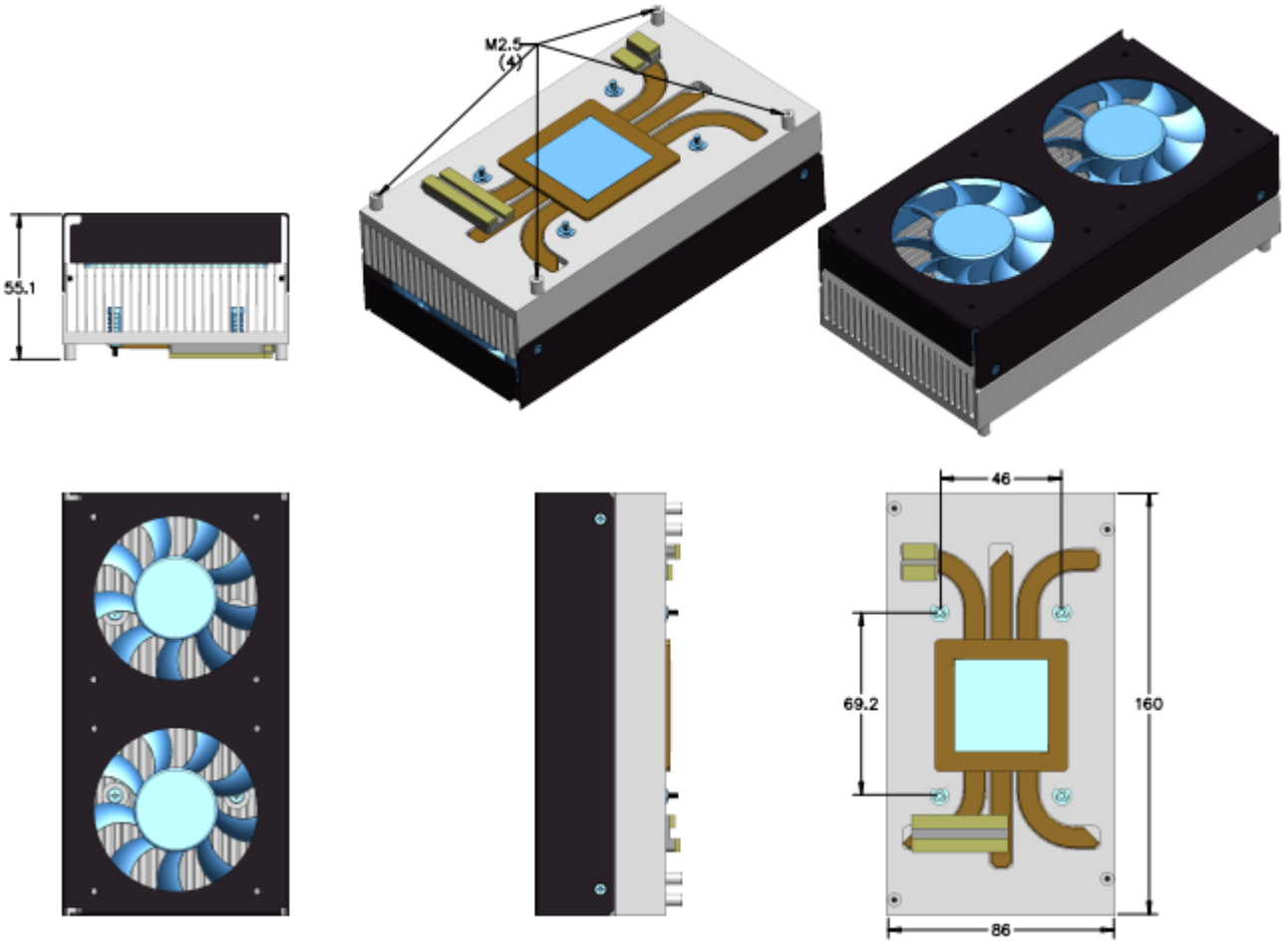


Figure 8 – Heatsink with Fan: THSF

11.1.4 Heatsink with Fan: THSF-BL-S

Dimensions: mm

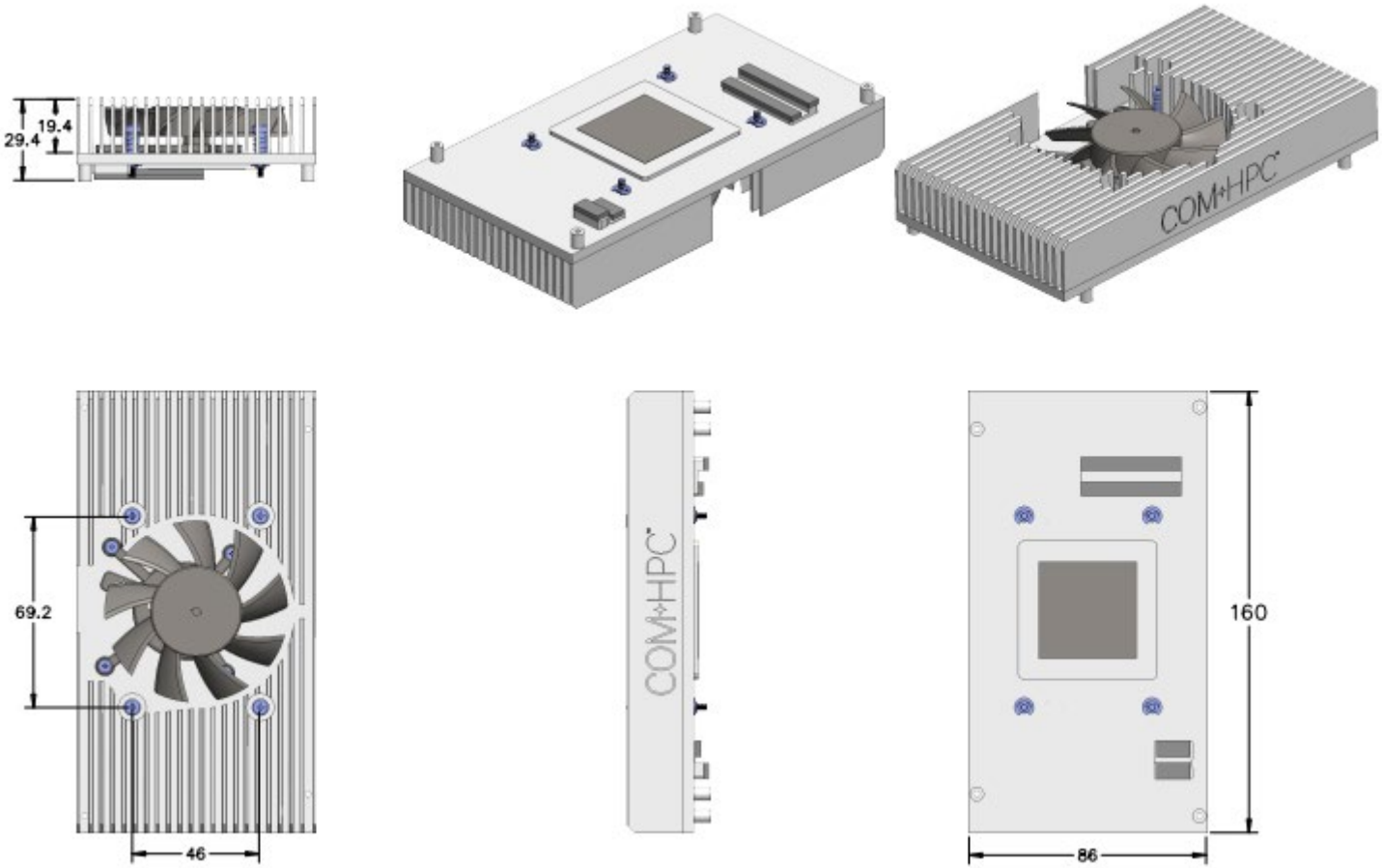


Figure 9 – Heatsink with Fan: THSF-BL-S