Express-ID7

User's Guide

intel

COM Express®

Revision: Rev. 1.0
Date: 2022-06-14
Part Number: 50M-00051-1000

ADLINK
LEADING EDGE COMPUTING

Revision History

Revision	Description	Date	Author
1.0	Initial release	2022-06-14	CC

Preface

Disclaimer

Information in this document is provided in connection with ADLINK products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in ADLINK´s Terms and Conditions of Sale for such products, ADLINK assumes no liability whatsoever, and ADLINK disclaims any express or implied warranty, relating to sale and/or use of ADLINK products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. If you intend to use ADLINK products in or as medical devices, you are solely responsible for all required regulatory compliance, including, without limitation, Title 21 of the CFR (US), Directive 2007/47/EC (EU), and ISO 13485 & 14971, if any. ADLINK may make changes to specifications and product descriptions at any time, without notice.

Environmental Responsibility

ADLINK is committed to fulfil its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

California Proposition 65 Warning: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks / registered trademarks of respective companies.

Copyright © 2022 ADLINK Technology Incorporated

Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

Getting Service

Ask an Expert: http://askanexpert.adlinktech.com

ADLINK Technology, Inc.
No. 66, Huaya 1st Rd., Guishan District, Taoyuan City 333411, Taiwan
Tel: +886-3-216-5088
Fax: +886-3-328-5706
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
6450 Via Del Oro, San Jose, CA 95119-1208, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-600-1189
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203, China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Strasse 11, D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

Please visit the Contact page at www.adlinktech.com for information on how to contact the ADLINK regional office nearest you.

Table of Contents

List of Figures

1. Introduction

The Express-ID7 is the first **COM Express® COM.0 R3.1 Basic Size Type 7** module based on the new generation and longevity, future-focused Intel® Xeon-D processors (formerly "Ice Lake D-1700") supporting up to 10 cores, extended operating temperature range for selected SKUs, and integrated 10G Ethernet connectivity, making it highly suited for mission-critical applications. Its 10 cores at 70 watts TDP combined with Intel® AVX-512 Vector Neural Network Instructions (VNNI) can optimize AI inferencing performance at the edge. Industries in need of such high performance, low power consumption, and high bandwidth connectivity include industrial automation and control, intelligent surveillance, video storage analytics, 5G infrastructure at the edge, and more.

The Express-ID7 features Intel® Virtualization Technology (including VT-x, VT-d), Intel® Hyper-Threading Technology, Intel® Trusted Execution Technology, Intel® AES-NI Technology, and up to 4 SO-DIMMs supporting a maximum of 128GB DDR4 ECC (or non-ECC) memory capacity with triple-channel memory design at up to 2933 MT/s (dependent on processor SKU) to provide excellent overall performance.

An integrated Intel® 10G Ethernet controller supports four 10GBASE-KR interfaces, with relevant sideband signals effectively reducing hardware and firmware complexity for system integration. The Express-ID7 is designed to serve customers requiring optimized computing capability per watt and high speed connectivity requirements who want to outsource the custom core logic of their systems for reduced development time.

Input/output features include 16 PCIe Gen4 lanes, 16 PCIe Gen3 lanes, a single onboard Gigabit Ethernet port with NC-SI, 4x USB 3.0/2.0 ports, and 2x SATA 6 Gb/s ports. Support for SMBus and I^2C is also provided. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

2. Specifications

2.1. Core System

CPU

Intel® Xeon® D-1700 Processor (formerly "Ice Lake D")

- Intel® Xeon® D-1746TER 2.0/3.1GHz, 15MB, 67W (10C/20T, eTEMP) (up to 2667 MT/s)
- Intel® Xeon® D-1735TR 2.2/3.4GHz, 15MB, 59W (8C/16T) (up to 2933 MT/s)
- Intel® Xeon® D-1732TE 1.9/3.0GHz, 15MB, 52W (8C/16T, eTEMP) (up to 2667 MT/s)
- Intel® Xeon® D-1715TER 2.4/3.5GHz, 10MB, 50W (4C/8T, eTEMP) (up to 2667 MT/s)
- Intel® Xeon® D-1712TR 2.0/3.1GHz, 10MB, 40W (4C/8T) (up to 2400 MT/s)

Note: Other non-IOTG SKUs (D-1748TE, D-1718T) and non-IOTG SKUs with Intel® QAT feature (D-1749NT, D-1747NTE, D-1736NT, D-1733NT, D-1734NT, D-1713NTE, D-1713NT) may be available by project basis.

Supporting: Intel® VT (including VT-x, VT-d, VT-x with Extended Page Tables), Intel® HT Technology, Intel® SSE4.2, Intel® 64 Architecture, Intel® Turbo Boost Technology 2.0, Intel® AVX512-VNNI, Intel® TSX-NI, Intel® Platform Protection Technology with Intel® TXT and Execute Disable Bit, Intel® Data Protection Technology with Intel® Secure Key and Intel® AES-NI (availability of features may vary between processor SKUs)

Memory

Up to 128GB DDR4, three memory channel in total four SODIMM sockets, maximum 32GB per socket, ECC or non-ECC

Up to 2933 MT/s memory speed (dependent on SKUs and 1DPC/2DPC usage)

Four SODIMM sockets supported by build option and project basis

Cache

15MB: D-1746TER, D-1735TR, D-1732TE

10MB: D-1715TER, D-1712TR

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 32 MB SPI BIOS, dual BIOS by build option

2.2. Expansion Busses

16 PCI Express Gen4: Lane 16-31 (four controllers, configurable to 1 x16, 2 x8, or 4 x4)
Refer to Ch. 4 Pinout and Signal Descriptions for details on Gen4 clock, PCIE_CK_REF1 (pin B29/B30)

8 PCI Express Gen3: Lanes 0-7 (four controllers, configurable to 1 x8, 2 x4, 4 x2/x1)

8 PCI Express Gen3: Lane 8-15 (four controllers, configurable to 1 x8, 2 x4, 4 x2/x1)

Note: Additional PCIe x1 at Lane 1 and Lane 5 are supported by build option and project basis.
PCIE_CK_REF (A88/A89) for Lane 16-31 (with up to Gen3 speed) is supported by build option and project basis.
Combined HSIO has a bandwidth up to the equivalent of 16 PCIe Gen3 lanes; PCIe lane 0-15, SATA, GbE and USB SSTX/RX are sourced from HSIO.

Other: SMBus (system), I^2C (user), LPC bus

2.3. 10G-KR Ethernet

Intel® Ethernet Controller integrated on SoC

Four 10GBASE-KR and sideband signals

PHY on carrier and ID EEPROM and PHY firmware are required for 10G SFP+ and/or Copper 10GBASE-T applications

The recommended PHY for SFP+ is C827, for 10GBASE-T is X557-AT4. The enablement of other PHY may require platform supplier support.

10G Ethernet Controller firmware is combined with BIOS code and stored on the same SPI ROM

10G Ethernet Controller firmware for 10K-KR backplane usage is different than that for 10G SFP+/10GBASE-T usage.

10G SFP+/10GBASE-T use the same firmware and are supported by default while 10G-KR backplane firmware is supported by build option and project basis.

Note: For detailed information about circuit design between the Ethernet controller, Optical Fiber/Copper PHY and firmware, please contact your local ADLINK representative
40GBASE-KR4 support requires the use of 4 KR lanes, which is supported by project basis (TBC).

2.4. GbE Ethernet

Intel® Ethernet Controller I210 Series

1000/100/10 Mbit/s connections

NC-SI and GBE0_SDP are supported on select SKU

2.5. Multi I/O and Storage

USB

4x USB 3.0/2.0/1.1 (USB 0, 1, 2, 3)

SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

USB_OC pins share the same source, from SOC

SATA

2x SATA 6Gb/s (SATA 0,1)

Note: Combined HSIO has a bandwidth up to the equivalent of 16 PCIe Gen3 lanes; PCIe lane 0-15, SATA, GbE and USB SSTX/RX are sourced from HSIO.

UART

Two UART interfaces SER0 and SER1 RX/TX on module
Console Redirection COM 1 or COM 2 selectable in BIOS

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	Yes

SER0, SER1 from SoC HSUART are supported by BOM option and project basis

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt, TBC)

2.6. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based)

2.7. SEMA Board Controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, flat panel control, general purpose I2C, failsafe BIOS (dual BIOS, opt. support), watchdog timer and fan control

2.8. Debug

30-pin flat cable connector for use with DB30 x86 debug module

Supports embedded controller access, SPI BIOS flashing, internal power rail test points, debug LEDs, and BIOS POST code LED

2.9. Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input: AT: 12V±5% or ATX: 12V±5% / 5Vsb ±5%

Power Management: ACPI 5.0 compliant

Power States: C0-C3, S0, S5, S5 ECO mode (WoL S5)

ECO Mode support for deep S5 for 5Vsb power saving

Note: For ATX power source, a minimum interval of 10ms is required from SUS_S3# fall to VCC_12V fall.

Power Consumption
Please contact your ADLINK representative for the document "COM Express Module Power Consumption".

2.10. Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.1 (COM.0 R3.1), Type 7, Basic size 125 x 95 mm

Operating Temperature

Standard	0°C to 60°C	Storage: -20°C to 80°C
Extreme Rugged	-40°C to 85°C	Storage: -40°C to 85°C (build option by project basis, selected SoC SKUs, TBC)

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

3. Block Diagram

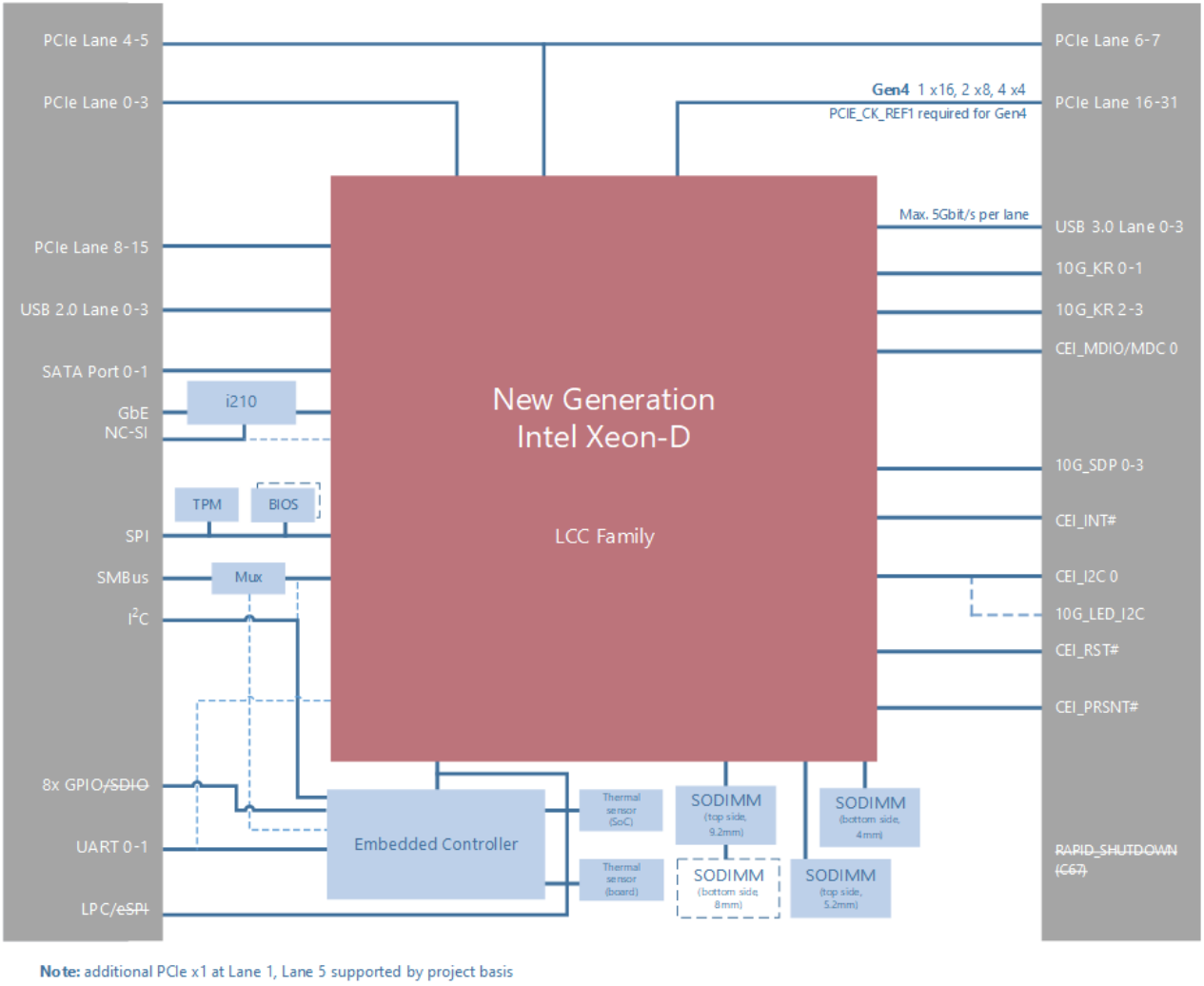


Figure 1 – Module functional block diagram

4. Pinout and Signal Descriptions

4.1. Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 7 in the PICMG COM.0 R3.1 specification. Signals described in the specification but not supported on the Express-ID7 are strikethrough ~~STRIKETHROUGH~~

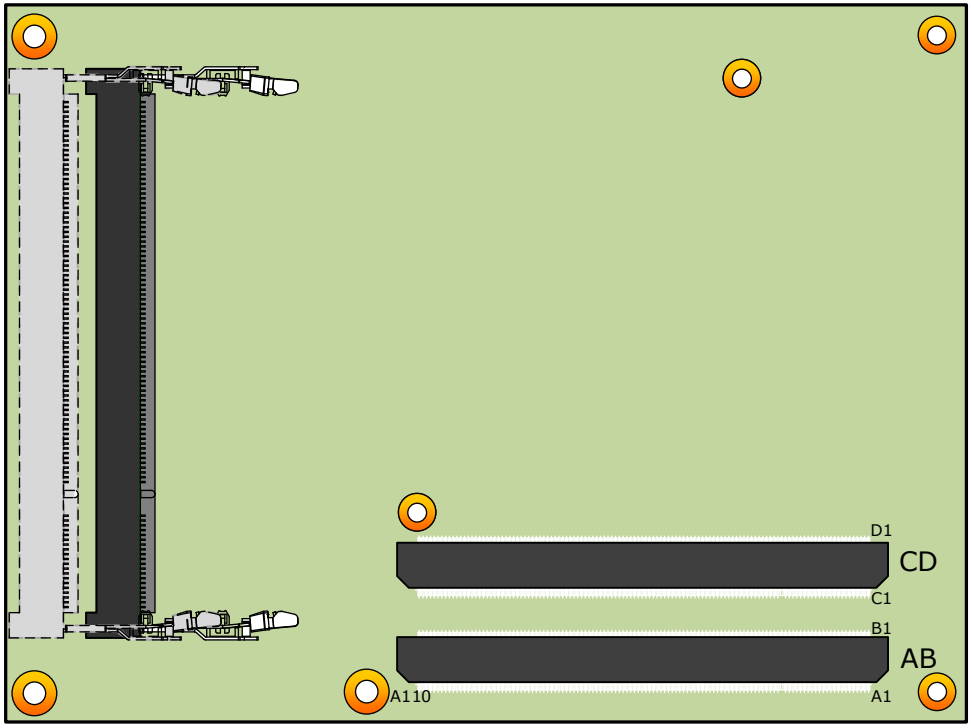


Figure 2 - Module rear side row and pin numbering

Note: The 4th SO-DIMM (grey color) is supported by build option.

Row A			Row B			Row C			Row D	
A1	GND (fixed)		B1	GND (fixed)		C1	GND (fixed)		D1	GND (fixed)
A2	GBE0_MDI3-		B2	GBE0_ACT#		C2	GND		D2	GND
A3	GBE0_MDI3+		B3	LPC_FRAME#		C3	USB_SSRX0-		D3	USB_SSTX0-
A4	GBE0_LINK100#		B4	LPC_AD0		C4	USB_SSRX0+		D4	USB_SSTX0+
A5	GBE0_LINK1000#		B5	LPC_AD1		C5	GND		D5	GND
A6	GBE0_MDI2-		B6	LPC_AD2		C6	USB_SSRX1-		D6	USB_SSTX1-
A7	GBE0_MDI2+		B7	LPC_AD3		C7	USB_SSRX1+		D7	USB_SSTX1+
A8	GBE0_LINK#		B8	~~LPC_DRQ0#~~		C8	GND		D8	GND
A9	GBE0_MDI1-		B9	~~LPC_DRQ1#~~		C9	USB_SSRX2-		D9	USB_SSTX2-
A10	GBE0_MDI1+		B10	LPC_CLK		C10	USB_SSRX2+		D10	USB_SSTX2+
A11	GND (fixed)		B11	GND (fixed)		C11	GND (fixed)		D11	GND (fixed)
A12	GBE0_MDI0-		B12	PWRBTN#		C12	USB_SSRX3-		D12	USB_SSTX3-
A13	GBE0_MDI0+		B13	SMB_CK		C13	USB_SSRX3+		D13	USB_SSTX3+
A14	GBE0_CTREF		B14	SMB_DAT		C14	GND		D14	GND
A15	SUS_S3#		B15	SMB_ALERT#		C15	~~10G_PHY_MDC_SCL3~~		D15	~~10G_PHY_MDIO_SDA3~~
A16	SATA0_TX+		B16	SATA1_TX+		C16	~~10G_PHY_MDC_SCL2~~		D16	~~10G_PHY_MDIO_SDA2~~
A17	SATA0_TX-		B17	SATA1_TX-		C17	10G_SDP2		D17	10G_SDP3
A18	SUS_S4#		B18	~~SUS_STAT#~~		C18	GND		D18	GND
A19	SATA0_RX+		B19	SATA1_RX+		C19	PCIE_RX6+		D19	PCIE_TX6+
A20	SATA0_RX-		B20	SATA1_RX-		C20	PCIE_RX6-		D20	PCIE_TX6-
A21	GND (fixed)		B21	GND (fixed)		C21	GND (fixed)		D21	GND (fixed)
A22	PCIE_TX15+		B22	PCIE_RX15+		C22	PCIE_RX7+		D22	PCIE_TX7+
A23	PCIE_TX15-		B23	PCIE_RX15-		C23	PCIE_RX7-		D23	PCIE_TX7-
A24	SUS_S5#		B24	PWR_OK		C24	~~10G_INT2~~		D24	~~10G_INT3~~
A25	PCIE_TX14+		B25	PCIE_RX14+		C25	GND		D25	GND
A26	PCIE_TX14-		B26	PCIE_RX14-		C26	10G_KR_RX3+		D26	10G_KR_TX3+
A27	BATLOW#		B27	WDT		C27	10G_KR_RX3-		D27	10G_KR_TX3-
A28	(S)ATA_ACT#		B28	**GND**		C28	GND		D28	GND
A29	RSVD		B29	**PCIE_CK_REF1+**		C29	10G_KR_RX2+		D29	10G_KR_TX2+
A30	RSVD		B30	**PCIE_CK_REF1-**		C30	10G_KR_RX2-		D30	10G_KR_TX2-
A31	GND (fixed)		B31	GND (fixed)		C31	GND (fixed)		D31	GND (fixed)
A32	RSVD		B32	SPKR		C32	~~10G_SFP_SDA3~~		D32	~~10G_SFP_SCL3~~
A33	RSVD		B33	I2C_CK		C33	~~10G_SFP_SDA2~~		D33	~~10G_SFP_SCL2~~
A34	BIOS_DIS0#		B34	I2C_DAT		C34	~~10G_PHY_RST_23~~		D34	~~10G_PHY_CAP_23~~
A35	THRMTRIP#		B35	THRM#		C35	~~10G_PHY_RST_01 /~~ **CEI_RST#**		D35	~~10G_PHY_CAP_01 /~~ **CEI_PRSNT#**

Row A			Row B			Row C			Row D	
A36	PCIE_TX13+		B36	PCIE_RX13+		C36	10G_LED_SDA *		D36	RSVD
A37	PCIE_TX13-		B37	PCIE_RX13-		C37	10G_LED_SCL *		D37	RSVD
A38	GND		B38	GND		C38	~~10G_SFP_SDA1~~		D38	~~10G_SFP_SCL1~~
A39	PCIE_TX12+		B39	PCIE_RX12+		C39	~~10G_SFP_SDA0 /~~ **CEI_SDA**		D39	~~10G_SFP_SCL0 /~~ **CEI_SCL**
A40	PCIE_TX12-		B40	PCIE_RX12-		C40	10G_SDP0		D40	10G_SDP1
A41	GND (fixed)		B41	GND (fixed)		C41	GND (fixed)		D41	GND (fixed)
A42	USB2-		B42	USB3-		C42	10G_KR_RX1+		D42	10G_KR_TX1+
A43	USB2+		B43	USB3+		C43	10G_KR_RX1-		D43	10G_KR_TX1-
A44	USB_2_3_OC#		B44	USB_0_1_OC#		C44	GND		D44	GND
A45	USB0-		B45	USB1-		C45	~~10G_PHY_MDC_SCL1~~		D45	~~10G_PHY_MDIO_SDA1~~
A46	USB0+		B46	USB1+		C46	~~10G_PHY_MDC_SCL0 /~~ **CEI_MDC**		D46	~~10G_PHY_MDIO_SDA0 /~~ **CEI_MDIO**
A47	VCC_RTC		B47	~~ESPI_EN#~~		C47	~~10G_INT0 /~~ **CEI_INT#**		D47	~~10G_INT1 /~~ **~~ETH0-3_PHY_INT#~~**
A48	RSVD		B48	~~USB0_HOST_PRSNT~~		C48	GND		D48	GND
A49	GBE0_SDP		B49	SYS_RESET#		C49	10G_KR_RX0+		D49	10G_KR_TX0+
A50	LPC_SERIRQ		B50	CB_RESET#		C50	10G_KR_RX0-		D50	10G_KR_TX0-
A51	GND (fixed)		B51	GND (fixed)		C51	GND (fixed)		D51	GND (fixed)
A52	PCIE_TX5+		B52	PCIE_RX5+		C52	PCIE_RX16+		D52	PCIE_TX16+
A53	PCIE_TX5-		B53	PCIE_RX5-		C53	PCIE_RX16-		D53	PCIE_TX16-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	RSVD
A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PCIE_RX17+		D55	PCIE_TX17+
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PCIE_RX17-		D56	PCIE_TX17-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PCIE_RX18+		D58	PCIE_TX18+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PCIE_RX18-		D59	PCIE_TX18-
A60	GND (fixed)		B60	GND (fixed)		C60	GND (fixed)		D60	GND (fixed)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PCIE_RX19+		D61	PCIE_TX19+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PCIE_RX19-		D62	PCIE_TX19-
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PCIE_RX20+		D65	PCIE_TX20+
A66	GND		B66	WAKE0#		C66	PCIE_RX20-		D66	PCIE_TX20-
A67	GPI2		B67	WAKE1#		C67	~~RAPID_SHUTDOWN~~		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PCIE_RX21+		D68	PCIE_TX21+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PCIE_RX21-		D69	PCIE_TX21-
A70	GND (fixed)		B70	GND (fixed)		C70	GND (fixed)		D70	GND (fixed)

Row A			Row B			Row C			Row D	
A71	PCIE_TX8+		B71	PCIE_RX8+		C71	PCIE_RX22+		D71	PCIE_TX22+
A72	PCIE_TX8-		B72	PCIE_RX8-		C72	PCIE_RX22-		D72	PCIE_TX22-
A73	GND		B73	GND		C73	GND		D73	GND
A74	PCIE_TX9+		B74	PCIE_RX9+		C74	PCIE_RX23+		D74	PCIE_TX23+
A75	PCIE_TX9-		B75	PCIE_RX9-		C75	PCIE_RX23-		D75	PCIE_TX23-
A76	GND		B76	GND		C76	GND		D76	GND
A77	PCIE_TX10+		B77	PCIE_RX10+		C77	RSVD		D77	RSVD
A78	PCIE_TX10-		B78	PCIE_RX10-		C78	PCIE_RX24+		D78	PCIE_TX24+
A79	GND		B79	GND		C79	PCIE_RX24-		D79	PCIE_TX24-
A80	GND (fixed)		B80	GND (fixed)		C80	GND (fixed)		D80	GND (fixed)
A81	PCIE_TX11+		B81	PCIE_RX11+		C81	PCIE_RX25+		D81	PCIE_TX25
A82	PCIE_TX11-		B82	PCIE_RX11-		C82	PCIE_RX25-		D82	PCIE_TX25-
A83	GND		B83	GND		C83	RSVD		D83	RSVD
A84	NCSI_TX_EN		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	PCIE_RX26+		D85	PCIE_TX26+
A86	RSVD		B86	VCC_5V_SBY		C86	PCIE_RX26-		D86	PCIE_TX26-
A87	RSVD		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	BIOS_DIS1#		C88	PCIE_RX27+		D88	PCIE_TX27+
A89	PCIE0_CK_REF-		B89	~~NSCI_RX_ER~~		C89	PCIE_RX27-		D89	PCIE_TX27-
A90	GND (fixed)		B90	GND (fixed)		C90	GND (fixed)		D90	GND (fixed)
A91	SPI_POWER		B91	NCSI_CLK_IN		C91	PCIE_RX28+		D91	PCIE_TX28+
A92	SPI_MISO		B92	NCSI_RXD1		C92	PCIE_RX28-		D92	PCIE_TX28-
A93	GPO0		B93	NCSI_RXD0		C93	GND		D93	GND
A94	SPI_CLK		B94	NCSI_CRS_DV		C94	PCIE_RX29+		D94	PCIE_TX29+
A95	SPI_MOSI		B95	NCSI_TXD1		C95	PCIE_RX29-		D95	PCIE_TX29-
A96	TPM_PP		B96	NCSI_TXD0		C96	GND		D96	GND
A97	TYPE10#		B97	SPI_CS#		C97	RSVD		D97	RSVD
A98	SER0_TX		B98	NCSI_ARB_IN		C98	PCIE_RX30+		D98	PCIE_TX30+
A99	SER0_RX		B99	NCSI_ARB_OUT		C99	PCIE_RX30-		D99	PCIE_TX30-
A100	GND (fixed)		B100	GND (fixed)		C100	GND (fixed)		D100	GND (fixed)
A101	SER1_TX		B101	FAN_PWMOUT		C101	PCIE_RX31+		D101	PCIE_TX31+
A102	SER1_RX		B102	FAN_TACHIN		C102	PCIE_RX31-		D102	PCIE_TX31-
A103	~~LID#~~		B103	~~SLEEP#~~		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V

Row A			Row B			Row C			Row D	
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (fixed)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Note: 10G SFP+ or 10GBASE-T support is based on CEI mode (sideband signal arrangement related) and requires PHY (C827 or X557-AT4) along with on-carrier firmware, for SFP+ or 10GBASE-T applications. A reference design will be offered. Please contact your ADLINK representative for availability

Note: Another PCIe clock (PCIE_CK_REF1) for up to Gen4 usage is required for PCIe lane 16-31. Check pin B28, B29, B30
To stay at PCIE_CK_REF and only needing up to Gen3 at PCIe lane 16-31, a build option on module to re-route the clock for lane 16-31 is supported by project basis

Note: 10G_LED_I2C (C36, C37) by build option supported by project basis.

Note: USB_0_1_OC# (B44) and USB_2_3_OC# (A44) share the same source, from Ice Lake D.

4.2. Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

4.3. AB Connector Signal Descriptions

4.3.1 Network Controller Sideband Interface (NC-SI)

Name	Pin #	Description	I/O	PU / PD	Comment
NCSI_CLK_IN	B91	Clock reference for receive, transmit and control interface	I 3.3VSB	PD 10K	
NCSI_RXD[1:0]	B92 B93	Receive Data (from NC to BMC)	O 3.3VSB	PU 10K 3.3VSB	PU 10K that aligns with LAN chip specification
NCSI_TXD[1:0]	B95 B96	Transmit Data (from BMC to NC)	I 3.3VSB	PU 10K 3.3VSB	
NCSI_CRS_DV	B94	Carrier Sense/Receive Data valid to MC, indicating that the transmitted data from NC to BMC is valid	O 3.3VSB	PD 10K	PU 10K that aligns with LAN chip specification
NCSI_TX_EN	A84	Transmit enable	I 3.3VSB	PD 10K	
~~NCSI_RX_ER~~	~~B89~~	~~Receive error~~	~~O~~ ~~3.3VSB~~		Not supported
NCSI_ARB_IN	B98	Network Controller hardware arbitration input	I 3.3VSB		Left floating on module, that aligns with LAN chip specification
NCSI_ARB_OUT	B99	Network Controller hardware arbitration output	O 3.3VSB		

Note: NC-SI source from Intel® Ethernet Controller I210.

4.3.2 Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK100# *	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_LINK1000# *	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.	REF GND min 3.3V max		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB	PU 10K 3.3VSB	Depends on the selection of LAN controller

Note: GBE0_ACT# and GBE0_LINK# share the same pin from LAN controller.

4.3.3 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 4.7K 3.3V	

4.3.3.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC	Comment
SATA0	HSIO 17	
SATA1	HSIO 19	

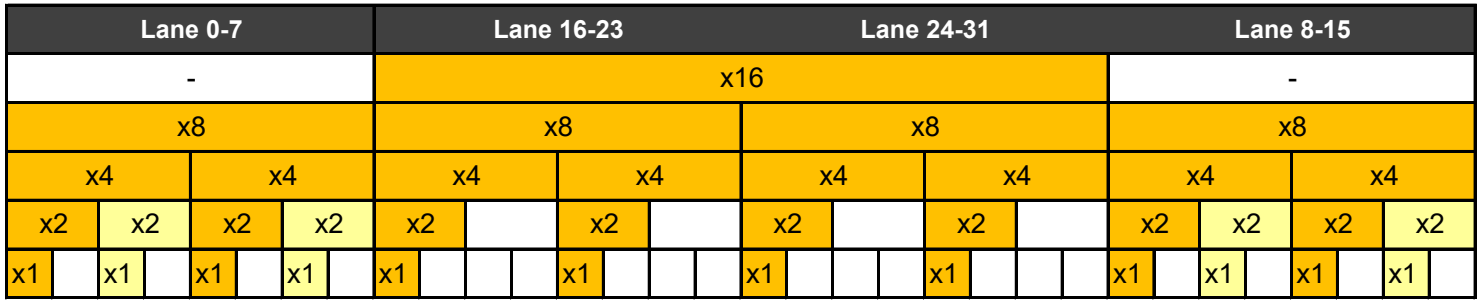
4.3.4 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX8+ PCIE_TX8-	A71 A72	PCI Express channel 8, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX8+ PCIE_RX8-	B71 B72	PCI Express channel 8, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX9+ PCIE_TX9-	A74 A75	PCI Express channel 9, Transmit Output differential pair.	O PCIE		AC coupled on Module

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_RX9+ PCIE_RX9-	B74 B75	PCI Express channel 9, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX10+ PCIE_TX10-	A77 A78	PCI Express channel 10, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX10+ PCIE_RX10-	B77 B78	PCI Express channel 10, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX11+ PCIE_TX11-	A81 A82	PCI Express channel 11, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX11+ PCIE_RX11-	B81 B82	PCI Express channel 11, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX12+ PCIE_TX12-	A39 A40	PCI Express channel 12, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX12+ PCIE_RX12-	B39 B40	PCI Express channel 12, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX13+ PCIE_TX13-	A36 A37	PCI Express channel 13, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX13+ PCIE_RX13-	B36 B37	PCI Express channel 13, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX14+ PCIE_TX14-	A25 A26	PCI Express channel 14, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX14+ PCIE_RX14-	B25 B26	PCI Express channel 14, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX15+ PCIE_TX15-	A22 A23	PCI Express channel 15, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX15+ PCIE_RX15-	B22 B23	PCI Express channel 15, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		
PCIE_CLK_REF1+ PCIE_CLK_REF1-	B29 B30		O PCIE		

Note: PCIE_CLK_REF1 (B29, B30) and GND (B28) are used for Gen4/3/2/1 speed at PCIe lane 16-31

PCI Express lane configuration as below



Compliant with PICMG definition

Additional configurations supported by Intel® Xeon® D platform.
Use caution when adopting these additional configurations.

Note: Additional PCIe x1 at Lane 1 and Lane 5 are by build option supported by project basis.

4.3.4.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC	Comment
PCIE0	HSIO 0	
PCIE1	HSIO 1	
PCIE2	HSIO 2	
PCIE3	HSIO 3	
PCIE4	HSIO 4	
PCIE5	HSIO 5	
PCIE6	HSIO 6	
PCIE7	HSIO 7	
PCIE8	HSIO 8	
PCIE9	HSIO 9	
PCIE10	HSIO 10	
PCIE11	HSIO 11	
PCIE12	HSIO 12	
PCIE13	HSIO 13	
PCIE14	HSIO 14	
PCIE15	HSIO 15	

4.3.5 LPC Bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3VSB	PU 10K 3.3VSB	This Intel platform requires PU
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB	PU 10K 3.3VSB	This Intel platform requires PU
~~LPC_DRQ0#~~ ~~LPC_DRQ1#~~	~~B8~~ ~~B9~~	~~LPC serial DMA request~~	~~I 3.3V~~		Not supported
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3VSB	PU 10K 3.3VSB	This Intel platform requires PU
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3VSB	PD 10K	The LPC_CLK frequency is 24MHz on this platform

4.3.6 USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
~~USB0_HOST_PRSNT~~	~~B48~~	~~Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.~~	~~I 3.3VSB~~		Not supported

***Note**: A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.

4.3.6.1. USB Root Segmentation

All USB interfaces are derived from the xHCI controller.

4.3.7 SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not connected

4.3.8 Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
~~SPKR~~	~~B32~~	~~Output for audio enunciator, the "speaker" in PC-AT systems~~	~~O 3.3V~~		Not supported
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10K 3.3V	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3VSB	PU 10K 3.3VSB	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100K	PD only when TPM on module. Modules implementing a TPM shall pull down

4.3.9 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Equivalent resistor is 2.2K
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Equivalent resistor is 2.2K
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 3.3V standby rail and main power rails.	I 3.3VSB	PU 10K 3.3VSB	

Note: SMBus source from SoC's SMBus is default setting. SMBus source from EC is by build option supported by project basis.

4.3.10 I2C Bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I^2C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)
I2C_DAT	B34	General purpose I^2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)

4.3.11 General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

4.3.12 Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 8.2K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 8.2K 3.3V	Power rail tolerance 5V, 12V

Note: SER0, SER1 source from EC is default setting. SER0, SER1 source from SoC's HSUART is by build option by supported by project basis. HSUART has driver support limitation.

4.3.13 Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Connect to SUS_S4#
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
~~LID#~~	~~A103~~	~~LID button. Low active signal used by the ACPI operating system for a LID switch.~~	~~I OD 3.3VSB~~		Not supported
~~SLEEP#~~	~~B103~~	~~Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.~~	~~I OD 3.3VSB~~		Not supported
~~RAPID_ SHUTDOWN~~	~~C67~~	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50-ohm source impedance for ≥ 20 µs.~~	~~I CMOS 5VSB~~		Not supported

4.3.14 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports wide range 5~ 20V input All available VCC_12V pins on the connector(s) shall be used.	P		12V ±5%
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B28, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

4.4. CD Connector Signal Descriptions

4.4.1 USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled off module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		AC coupled off module
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on module

4.4.1.1. USB Root Segmentation

All USB interfaces are derived from the xHCI controller.

4.4.2 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		AC coupled off Module

4.4.2.1. PCH HSIO Lane Assignments

Refer to section **4.3.4.1 PCH HSIO Lane Assignments** for detailed info.

4.4.3 10G-KR Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
10G_KR_RX0+ 10G_KR_RX0- 10G_KR_RX1+ 10G_KR_RX1-	C49 C50 C42 C43	10GBASE-KR ports, Receive Input differential pairs	I KR		AC coupled on Module
10G_KR_TX0+ 10G_KR_TX0- 10G_KR_TX1+ 10G_KR_TX1-	D49 D50 D42 D43	10GBASE-KR ports, Transmit Output differential pairs	O KR		AC coupled on Carrier
10G_KR_RX2+ 10G_KR_RX2- 10G_KR_RX3+ 10G_KR_RX3-	C29 C30 C26 C27	10GBASE-KR ports, Receive Input differential pairs	I KR		AC coupled on Module
10G_KR_TX2+ 10G_KR_TX2- 10G_KR_TX3+ 10G_KR_TX3-	D29 D30 D26 D27	10GBASE-KR ports, Transmit Output differential pairs	O KR		AC coupled on Carrier
~~10G_INT0 /~~ **CEI_INT#**	C47	Interrupt pin from Copper PHY or Optical SFP+ module to the 10GbE controller	I 3.3VSB	PU 10K 3.3VSB	This pin is used for CEI mode
~~10G_INT1~~ ~~10G_INT2~~ ~~10G_INT3~~	~~D47~~ ~~C24~~ ~~D24~~	~~Interrupt pin from Copper PHY or Optical SFP+ module to the 10GbE controller~~	~~I 3.3VSB~~		Not supported
~~10G_PHY_MDIO_SDA0~~ ~~/~~ **CEI_MDIO**	D46	MDIO mode Management Data I/O Interface mode data signal for serial data transfers between the MAC and an external PHY ~~I2C mode~~ ~~I2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY~~	I/O 3.3VSB	PU 1K 3.3VSB	This pin is used for CEI mode

Name	Pin #	Description	I/O	PU / PD	Comment
~~10G_PHY_MDC_SCL0~~ / **CEI_MDC**	C46	MDIO mode Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY ~~I2C mode~~ ~~I2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY~~	O 3.3VSB	PU 1K 3.3VSB	This pin is used for CEI mode
~~10G_PHY_MDIO_SDA1~~ ~~10G_PHY_MDIO_SDA2~~ ~~10G_PHY_MDIO_SDA3~~	~~D45~~ ~~D16~~ ~~D15~~	~~MDIO mode~~ ~~Management Data I/O Interface mode data signal for serial data transfers between the MAC and an external PHY~~ ~~I2C mode~~ ~~I2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY~~	~~O 3.3VSB~~ ~~I/O OD 3.3VSB~~		Not supported
~~10G_PHY_MDC_SCL1~~ ~~10G_PHY_MDC_SCL2~~ ~~10G_PHY_MDC_SCL3~~	~~C45~~ ~~C16~~ ~~C15~~	~~MDIO mode~~ ~~Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY~~ ~~I2C mode~~ ~~I2C Data signal, of the 2-wire management interface used for serial data transfers between the MAC and the external PHY~~	~~O 3.3VSB~~ ~~I/O OD 3.3VSB~~		Not supported
10G_SDP0 10G_SDP1 10G_SDP2 10G_SDP3	C40 D40 C17 D17	Software-Definable Pins	I/O 3.3VSB	PU 20K 3.3VSB	This Intel platform requires PU
~~10G_SFP_SDA0 /~~ **CEI_SDA**	C39	I2C Data signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module	I/O OD 3.3VSB	PU 10K 3.3VSB	This pin is used for CEI mode
~~10G_SFP_SCL0 /~~ **CEI_SCL**	D39	I2C Clock signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module	I/O OD 3.3VSB	PU 10K 3.3VSB	This pin is used for CEI mode

Name	Pin #	Description	I/O	PU / PD	Comment
~~10G_SFP_SDA1~~ ~~10G_SFP_SDA2~~ ~~10G_SFP_SDA3~~	~~C38~~ ~~C33~~ ~~C32~~	~~I2C Data signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module~~	~~I/O OD 3.3VSB~~		Not supported
~~10G_SFP_SCL1~~ ~~10G_SFP_SCL2~~ ~~10G_SFP_SCL3~~	~~D38~~ ~~D33~~ ~~D32~~	~~I2C Clock signal, of the 2-wire management interface used by 10GbE controller to access the management registers of an external Optical SFP+ module~~	~~I/O OD 3.3VSB~~		Not supported
~~10G_PHY_RST_01 /~~ **CEI_RST#**	C35	Output signal that resets and Optical PHY on port 0 and port 1	O 3.3VSB	PD 10K	This pin is used for CEI mode
~~10G_PHY_RST_23~~	~~C34~~	~~Output signal that resets and Optical PHY on port 0 and port 1~~	~~O 3.3VSB~~		Not supported
~~10G_PHY_CAP_01 /~~ **CEI_PRSNT#**	D35	Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface	I 3.3VSB	PU 10K 3.3VSB	This pin is used for CEI mode
~~10G_PHY_CAP_23~~	~~D34~~	~~Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface~~	~~I 3.3VSB~~	~~PU 10K 3.3VSB~~	Not supported
10G_LED_SDA	C36	I2C Data signal, of the 2-wire that transfers all LED signals and additional Strapping signal for I2C or MDIO mode of Optical PHY	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Build option by project basis
10G_LED_SCL	C37	I2C Clock signal, of the 2-wire that transfers all LED signals and additional Strapping signal for I2C or MDIO mode of Optical PHY	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Build option by project basis

Note: For detailed information about circuit design between the Ethernet controller, Optical Fiber/Copper PHY and firmware, please contact your local ADLINK representative.

4.4.4 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express channel 16, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express channel 16, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express channel 17, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express channel 17, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express channel 18, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express channel 18, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express channel 19, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express channel 19, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express channel 20, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express channel 20, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express channel 21, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express channel 21, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express channel 22, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express channel 22, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express channel 23, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express channel 23, Receive Input differential pair.	I PCIE		AC coupled off Module

PCIE_TX24+ PCIE_TX24-	D78 D79	PCI Express channel 24, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX24+ PCIE_RX24-	C78 C79	PCI Express channel 24, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX25+ PCIE_TX25-	D81 D82	PCI Express channel 25, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX25+ PCIE_RX25-	C81 C82	PCI Express channel 25, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX26+ PCIE_TX26-	D85 D86	PCI Express channel 26, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX26+ PCIE_RX26-	C85 C86	PCI Express channel 26, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX27+ PCIE_TX27-	D88 D89	PCI Express channel 27, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX27+ PCIE_RX27-	C88 C89	PCI Express channel 27, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX28+ PCIE_TX28-	D91 D92	PCI Express channel 28, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX28+ PCIE_RX28-	C91 C92	PCI Express channel 28, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX29+ PCIE_TX29-	D94 D95	PCI Express channel 29, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX29+ PCIE_RX29-	C94 C95	PCI Express channel 29, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX30+ PCIE_TX30-	D98 D99	PCI Express channel 30, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX30+ PCIE_RX30-	C98 C99	PCI Express channel 30, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX31+ PCIE_TX31-	D101 D102	PCI Express channel 31, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX31+ PCIE_RX31-	C101 C102	PCI Express channel 31, Receive Input differential pair.	I PCIE		AC coupled off Module

Note: PCIE_CLK_REF1 (B29, B30) and GND (B28) are used for Gen4/3/2/1 speed at PCIe lane 16-31.
If up to Gen3 speed is required on PCIe lane 16-31 and would like to use PCIe clock from A88/A89, a build option on the module can be supported by project basis.

4.4.5 Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10 that lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The Carrier Board ***should*** implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.			Type 7
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			No PD

4.4.6 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports wide range 5~ 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		12V ±5%
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

5. Additional Features

This chapter describes connectors, LEDs, switches and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items are shown below:

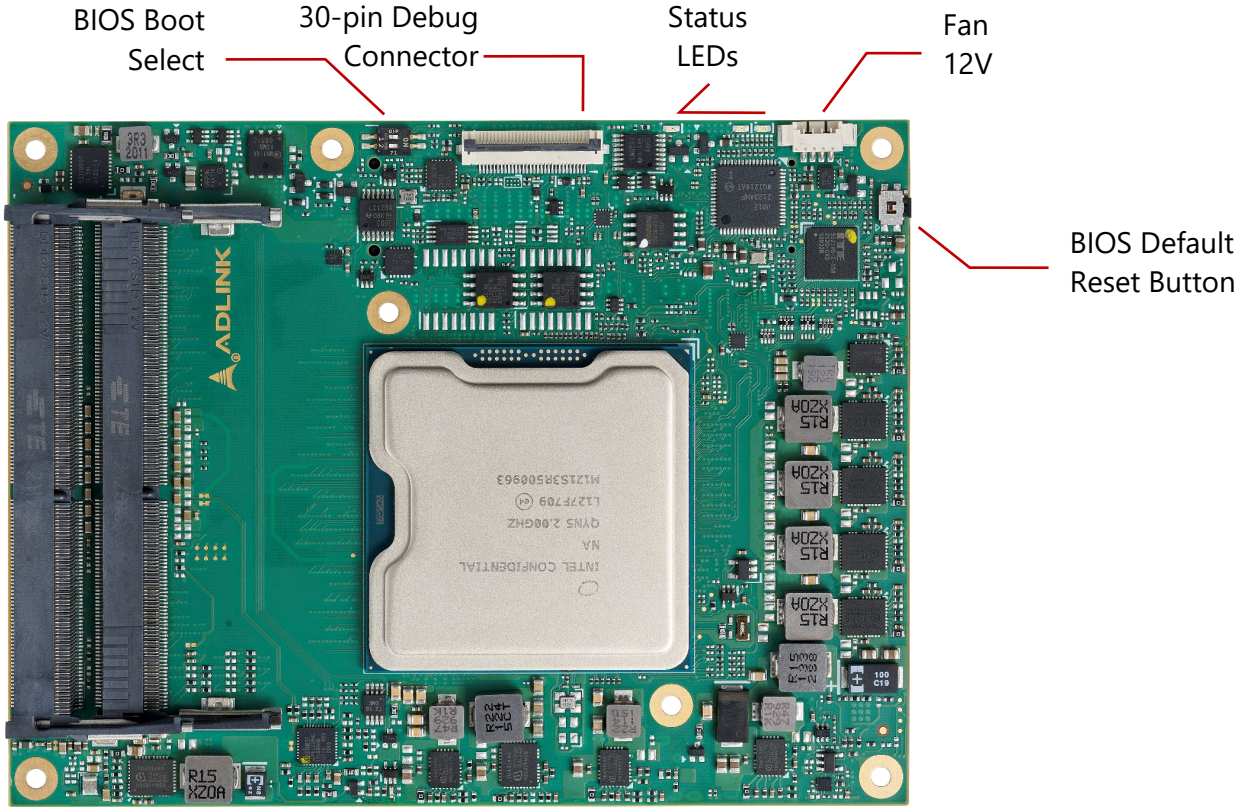


Figure 3 – Module feature locations

5.1. Debug Connector

This connector is particular useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points measurement of internal power rails
- I2C bus for BIOS POST code readout
- SPI BIOS programming interface
- Embedded Controller programming interface

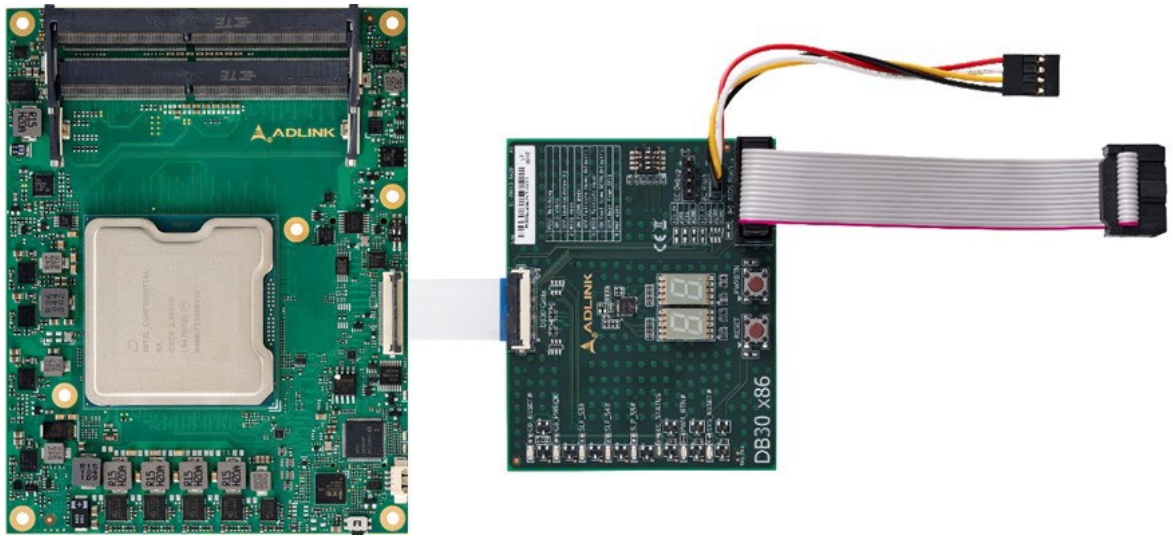


Figure 4 – Express-ID7 and Debug Module

5.2. Status LEDs

Status LED's are mounted on the module to facilitate easier maintenance.

LED3 LED2 LED1

Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: Only a RESET not initiated by the BMC can clear the WD LED (user action)

5.3. Exception Codes

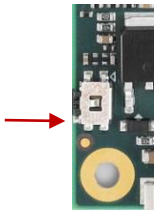
Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
8	RESETIN_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
15	NO_V1P05A_PG
16	NO_VCORE_PG
17	NO_SYS_GD
18	NO_V5SBY
19	NO_V3P3A
20	NO_V5_DUAL
21	NO_PWRSRC_GD
22	NO_P_5V_3V3_S0_PG
23	NO_SAME_CHANNEL
24	NO_PCH_PG

5.4. Fan Connector

Connector type: JVE 24W1125A-04M00

Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

5.5. BIOS Default Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Keep the BIOS Setup Defaults Reset Button pressed and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.

5.6. BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

6. BIOS Checkpoints, Beep Codes

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to a following initialization step. Error codes signify error conditions encountered in the process of system initialization. The Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but the Aptio 5.x core can be configured to send checkpoints to a variety of sources. The Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. A beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not the only sounds generated during the boot process. Some firmware components may use sounds to notify the user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes

Viewing Checkpoints

Checkpoints generated by the Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-on cards show the value of I/O port 80h on an LED display.

Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

7. Software Support

7.1.1 Windows Server 2019, Windows 10 IoT Enterprise LTSC

Windows Server 2022 is scheduled to be supported in Q4.

7.1.2 Yocto Linux

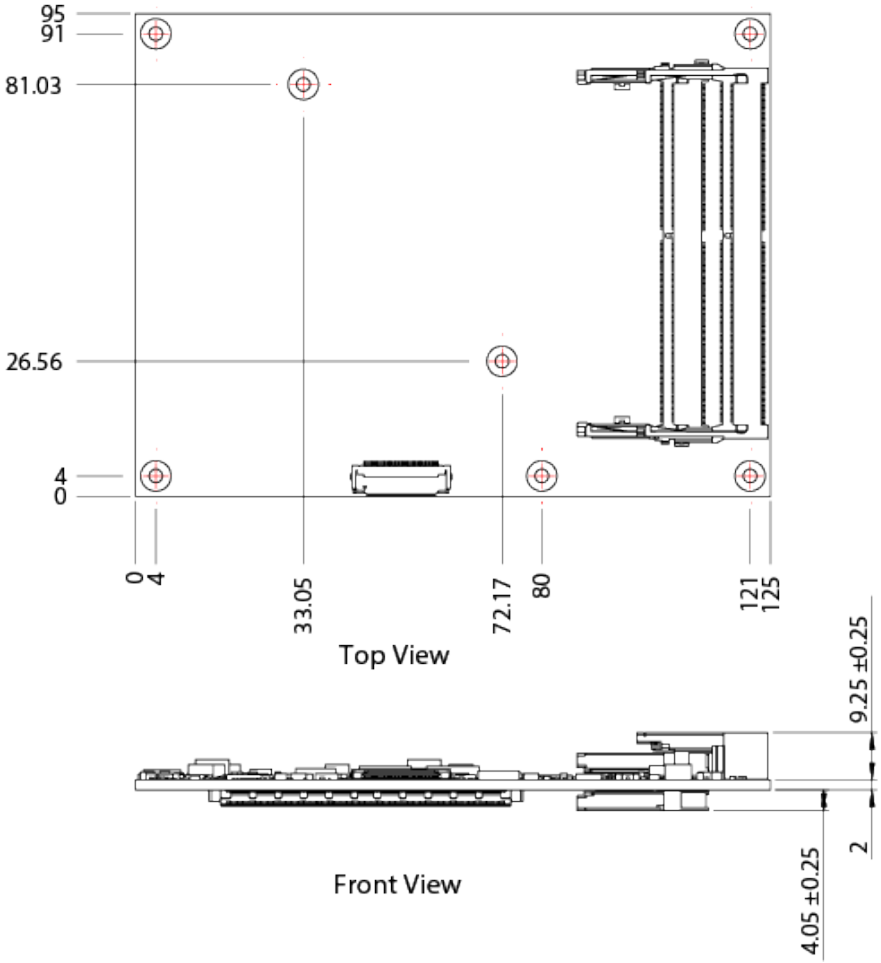
Yocto is scheduled to be supported in Q3

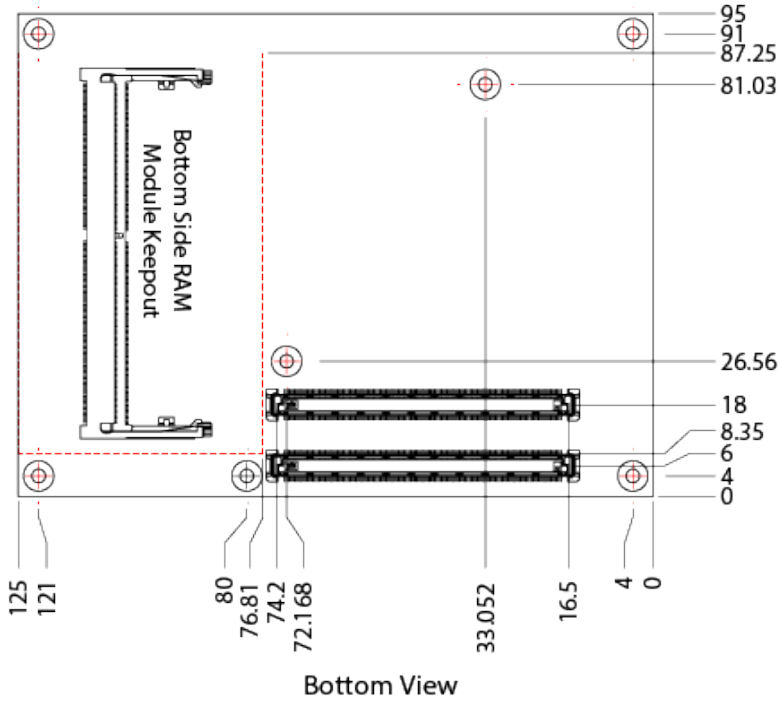
7.1.3 VxWorks

VxWorks is scheduled to be supported in Q3

8. Mechanical and Thermal

8.1. Module Dimensions





All dimensions are shown in millimeters. Tolerances should be ± 0.25mm, unless otherwise noted.
The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00]&[16.50,18.00]) should be ± 0.10mm.

Dimensions: mm

Figure 5 – Module mechanical dimensions

8.2. Thermal Solutions

8.2.1 Heatspreader: HTS

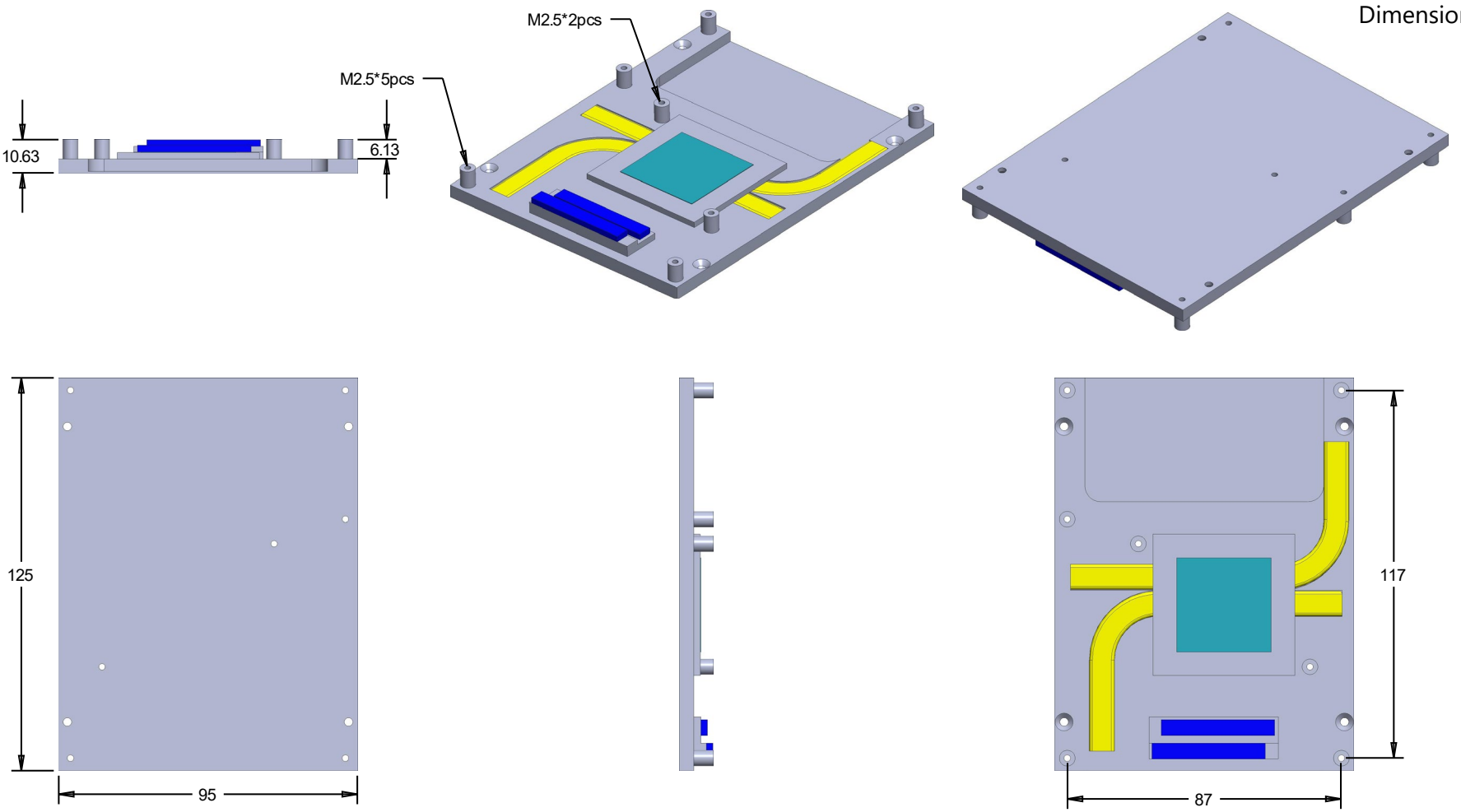


Figure 6 – Heatspreader HTS

8.2.2 Heatsink with Fan: THSF

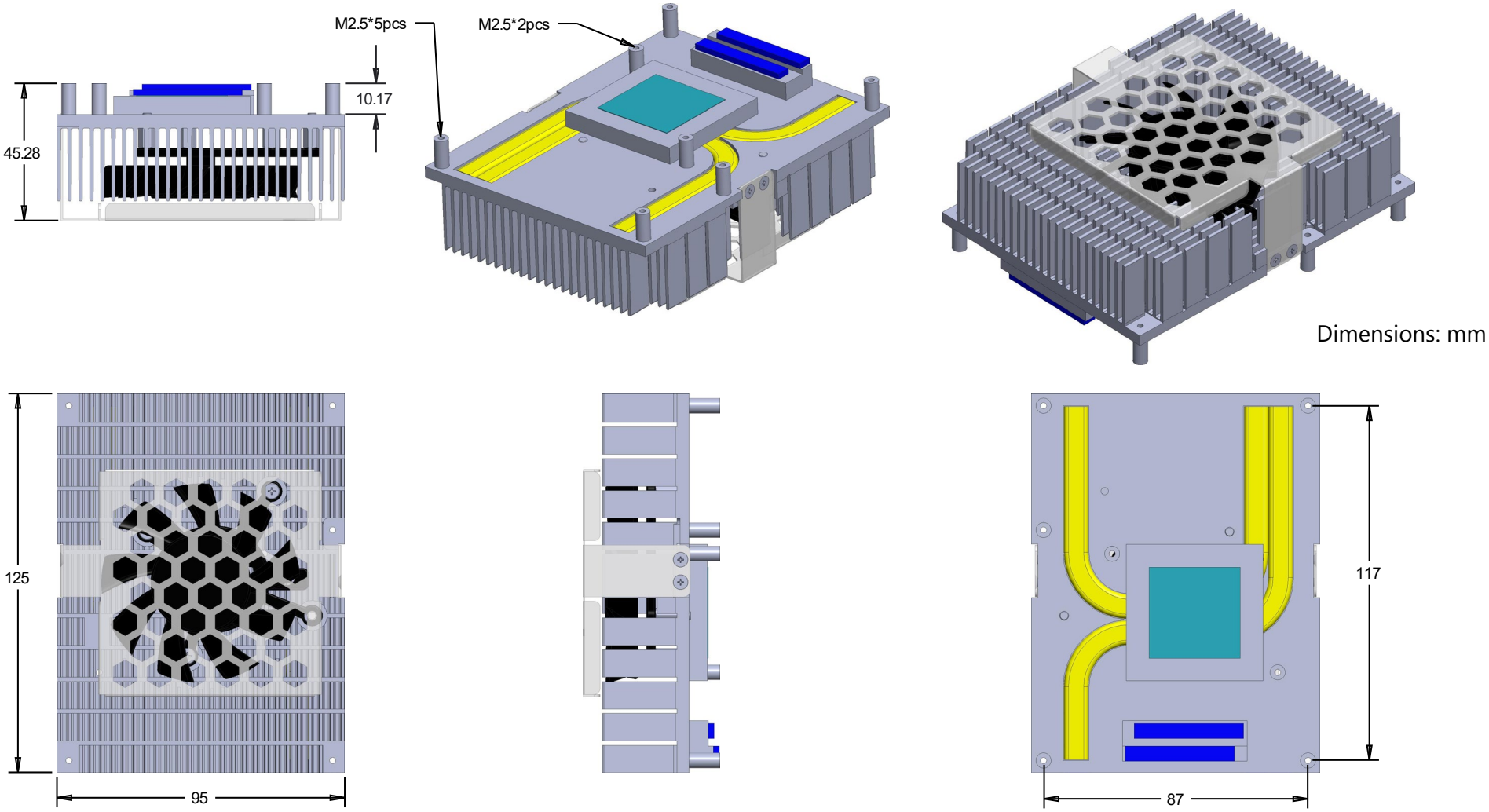


Figure 7 – Heatsink with Fan: THSF